PANEL DISCUSSION DURING SPIE 2024

February 26, 2024 at 7:00 PM PT
Marriott Hotel, San Jose

JUNKO YOSHIDA

Editor-in-Chief,
The Ojo-Yoshida Report

Junko cut her teeth as a roving reporter in Tokyo, Silicon Valley, Paris, New York and more recently in China to find exclusive/breaking stories and write incisive analysis. During her time as bureau chief and editor-in-chief of EE Times, she developed a good understanding of the inner workings of the semiconductor industry.

Her time as global EiC also taught her the importance of providing a differentiated offering for the Ojo-Yoshida Report. Most newsletters dispense news. OYR offers analysis of the news and provides answers to the questions everyone has: How will what is happening in the semiconductor industry affect them?

The many lasting relationships Junko has developed over the course of her career enhance her ability to break down complex information, make sense of specific industry news and extrapolate what is driving the trends and the impact they will have.

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STEVEN SCHEER

Vice President
Advanced Patterning Process and Materials
Imec

Steven Scheer has been the Senior Vice President of Advanced Patterning Process and Materials (APPM) at imec since January 2019. His responsibilities include patterning, unit process and new materials development for logic, memory, photonics, and 3D integration. Prior to that, he was an account technology director with Tokyo Electron Ltd. (TEL), responsible for customers in the Portland OR area. He worked at TEL for 13 years where he was responsible for R&D in patterning and cleans, including management roles in the US as well as at TEL's factory in Kumamoto Japan and with the corporate R&D organization in Tokyo. He began his research career at IBM in Fishkill NY, working on 90 and 65 nm patterning development. He holds a Ph.D. in Chemical Engineering from the University of Texas at Austin.

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MARK PHILIPS

Fellow
Intel

Mark Phillips is an Intel Fellow in the Technology and Manufacturing Group and the director of lithography hardware and solutions at Intel Corporation. He is responsible for working with Intel's lithography equipment suppliers to maintain a pipeline of new tools and technologies that support the patterning requirements of future Intel process technologies. Mark joined Intel in 1993 to work on the development of 0.35-micron process technology. During his tenure at Intel, Mark has contributed to every generation of lithography exposure tool, from i-line steppers to 193-nanometer (193nm) immersion scanners, EUV scanners, and now high NA EUV scanners. In recent years, he has also managed the groups responsible for Intel's lithography metrology development. He was appointed an Intel Fellow in 2016, and an SPIE Fellow also in 2016.

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KUMARA SASTRY

Engineer
NVIDIA

Kumara Sastry is a Distinguished Engineer in the Advanced Technology Group at NVIDIA, working on computational methods for advanced semiconductor manufacturing. Previously, he worked at Intel till 2021 on Computational Lithography and AI-based Metrology, last serving as Senior Director. He got his bachelor's from BITS Pilani in India, and his PhD from the University of Illinois at Urbana Champaign in 2007. He has over 50 publications, over 6000 citations and 16 patents published or pending. In addition to being a regular participant at SPIE Advanced Lithography, Kumara is also a Member of the Board of the Lithography Workshop.

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STEFFEN SCHULZE

Vice President
Siemens EDA

Steffen Schulze is currently the Vice President of Product Management in the Design to Silicon Division at Siemens EDA within the Siemens Digital Industries Software organization. His group manages the product development activities for all semiconductor manufacturing software tools in the Calibre product line. Steffen holds a Master's degree in Material Science from the Institute for Fine Chemical Technology M.W. Lomonossov, Moscow, Russia; a Ph.D. in Electrical Engineering from the University of Bremen, Germany; and an MBA from the University of Oregon in Eugene, Oregon USA.

Steffen started his professional career focused on technology development in mask manufacturing in the mask house at the Center of Microelectronics in Dresden, Germany. He led the ramp up of a new manufacturing facility for ebeam lithography and proceeded to take ownership of the customer facing data preparation group. He later worked for four years developing projects for micro-mechanical systems at the Institute for Microsensors, Actuators and Systems in Bremen, Germany, where he ran the lithography laboratory and was in charge of the mask design activities. In 1997 Steffen joined Infineon Technologies at the DRAM Alliance with IBM in East Fishkill, New York USA. His work focused on mask data preparation and advanced resolution enhancement techniques. In 2002 Steffen joined Mentor Graphics leading the launch of the Calibre MDP product line. Subsequently his activities expanded to improving the efficiency of the entire post tapeout flow in foundries and IDMs. His current responsibility is leading product development efforts of advanced tools in modeling, mask synthesis, resolution enhancement, mask data preparation, defect management and yield enhancement for semiconductor manufacturing customers. Steffen has over 50 publications and holds 9 patents.

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REGINA FREED

Vice President
Applied Materials

Regina Freed has more than 20 years of experience in the semiconductor industry, managing semiconductor process and equipment development for both logic and memory processes, including co-optimization between deposition and etch, lithography, metrology, and defect inspection. At Applied Materials, Regina leads our AIx™ program that enables us and our customers to accelerate development and ramp through Actionable Insights as well as control our processes to deliver improved process windows, enabling customers to scale faster and at lower cost, while optimizing device performance.

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