Applied Materials Leads the Drive to Accelerate TSV Adoption in 3-Dimensional ICs

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SANTA CLARA, Calif., Dec 01, 2008 (BUSINESS WIRE) -- Applied Materials, Inc. today announced that it is leading a major effort to enable the widespread adoption of through-silicon vias (TSVs), a rapidly-emerging approach for vertically stacking integrated circuits (ICs) to boost chip performance and functionality in a smaller area. TSVs will be critical to satisfying consumers' demands for faster, smaller electronics, enabling applications such as DDR4 DRAM memories and future communications and mobile internet chips. Since the biggest roadblock to implementing TSVs is cost, Applied is working internally and with other equipment suppliers to develop an integrated, high-performance on-wafer process flow to lower the cost, reduce the risk and accelerate time to market for customers.

Three-dimensional (3-D) IC integration is a new way for chip designers to deliver higher density, lower power consumption devices in a smaller footprint--without necessarily scaling the technology node. By modifying conventional wafer processing and packaging steps, multiple layers of similar or varying 2-D devices are stacked and interconnected using TSVs so they function as a single device--thus avoiding the cost, space and performance issues associated with combining multiple functions on one chip.

There are several approaches to TSV implementation, and Applied has the production-proven 300mm systems and processes required for the majority of TSV manufacturing steps, including mask, etch, film deposition and CMP* technologies. For example, the simultaneously announced Applied Centura(R) Silvia(TM) etch system was designed specifically to enable high-performance, low-cost TSV applications. To accelerate mainstream adoption, Applied is working with other equipment suppliers, such as Semitool, Inc. and wafer bonders, to fully characterize inter-process dependencies while lowering overall costs.

The value of TSV-enabled products is expected to increase significantly based on their enhanced performance that will in turn offset the increased cost of manufacturing. The EMC-3D Consortium of equipment suppliers estimates this cost target to be $190 per wafer; Applied's goal is to reduce this cost to less than $150 per wafer.

"TSV technology will revolutionize chip designs and has great potential to expand into more sophisticated integrated memory/logic applications. Our collaboration with other equipment suppliers is an innovative way of doing business that is beneficial for the industry and can solve our customers' problems," said Hans Stork, group vice president and CTO of Applied's Silicon Systems Group. "The capability to validate complete process flows at our Maydan Technology Center gives us a unique window into how we can lower the cost and mitigate customer risk in adopting TSV processes. By providing the technology and key supplier relationships, we can help accelerate the adoption of TSVs for mainstream manufacturing."

Applied Materials, Inc. (Nasdaq:AMAT) is the global leader in Nanomanufacturing Technology(TM) solutions with a broad portfolio of innovative equipment, service and software products for the fabrication of semiconductor chips, flat panel displays, solar photovoltaic cells, flexible electronics and energy efficient glass. At Applied Materials, we apply Nanomanufacturing Technology to improve the way people live. Learn more at www.appliedmaterials.com.

*CMP: chemical mechanical planarization

SOURCE: Applied Materials, Inc.

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