



Applied Materials Enables Cost-Effective Vertical Integration of 3D Chips

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- *Endura® Ventura(TM) PVD system allows high aspect ratio through-silicon via (TSV) structures for copper interconnects while reducing cost of ownership by up to 50 percent*
- *Industry's first high-volume manufacturing PVD titanium barrier solution for improved TSV reliability*

SANTA CLARA, Calif., May 28, 2014 - Applied Materials, Inc. today introduced the [Endura® Ventura\(TM\) PVD system](#) that helps customers reduce the cost of fabricating smaller, lower power, high-performance integrated 3D chips. The system incorporates Applied's latest innovations to its industry-leading PVD* technology that enables the deposition of thin, continuous barrier and seed layers in through-silicon-vias (TSVs). Demonstrating Applied's precision materials engineering expertise, the Ventura system also uniquely supports the use of titanium in volume production as an alternate barrier material for lower cost. With the launch of the Ventura system, Applied is expanding its comprehensive toolset for wafer level packaging (WLP) applications, including TSVs, redistribution layer (RDL) and Bump*.

TSVs are a critical technology for vertically fabricating smaller and lower power future mobile and high-bandwidth devices. Vias are short vertical interconnects that pass through the silicon wafer, connecting the active side of the device to the back side of the die, providing the shortest interconnect path between multiple chips. Integrating 3D stacked devices requires greater than 10:1 aspect ratio TSV interconnect structures to be metallized with copper. The new Ventura tool solves this challenge with innovations in materials and deposition technology to manufacture TSVs more cost-effectively than previous industry solutions.

"Building on 15 years of leadership in copper interconnect technology, the Ventura system enables fabrication of robust high-aspect ratio TSVs, with up to 50 percent barrier seed cost savings compared to copper interconnect PVD systems," said Dr. Sundar Ramamurthy, vice president and general manager of [Metal Deposition Products](#) at Applied Materials. "These innovations deliver a higher-performance and more functional, yet, compact chip package with less power consumption to meet leading-edge computing needs. Customers are realizing the benefits of this new PVD system and are qualifying it for volume manufacturing."

Supporting the manufacture of high-yielding 3D chips, the Ventura system introduces advances in ionized PVD technology that assure the integrity of the barrier and seed layers that are critical to superior gap-fill and interconnect reliability. These developments significantly improve ion directionality to enable the deposition of thin, continuous and uniform metal layers deep into the vias to achieve the void-free fill necessary for robust TSVs. With the improvement in directionality, higher deposition rates can be achieved, while the amount of barrier and seed material needed can be reduced. These attributes of the Ventura system and the adoption of titanium as an alternate barrier are expected to improve device reliability and reduce the overall cost of ownership for TSV metallization.

Applied Materials, Inc. (Nasdaq:AMAT) is the global leader in providing innovative equipment, services and software to enable the manufacture of advanced semiconductor, flat panel display and solar photovoltaic products. Our technologies help make innovations like smartphones, flat screen TVs and solar panels more affordable and accessible to consumers and businesses around the world. Learn more at www.appliedmaterials.com.

*PVD = physical vapor deposition

*Under Bump Metallization = used to connect the die to substrate

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[PHOTO: Applied Materials Endura® Ventura™ PVD system](#)

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