Applied Materials Breakthrough in Chip Wiring Enables Logic Scaling to 3nm and Beyond

June 16, 2021

- *Integrating seven process technologies in one system under vacuum cuts interconnect resistance in half*
- *New materials engineering approaches increase chip performance and reduce power consumption*
- *Latest system exemplifies Applied's strategy to be the PPACt enablement company™ for customers*

SANTA CLARA, Calif., June 16, 2021 (GLOBE NEWSWIRE) -- Applied Materials, Inc. today unveiled a new way to engineer the wiring of advanced logic chips that enables scaling to the 3nm node and beyond.

While size reduction benefits transistor performance, the opposite is true in the interconnect wiring: smaller wires have greater electrical resistance which reduces performance and increases power consumption. Without a materials engineering breakthrough, interconnect via resistance would increase by a factor of 10 from the 7nm node to the 3nm node, negating the benefits of transistor scaling.

Applied Materials has developed a new materials engineering solution called the Endura® Copper Barrier Seed IMS™. It is an Integrated Materials Solution that combines seven different process technologies in one system under high vacuum: ALD, PVD, CVD, copper reflow, surface treatment, interface engineering and metrology. The combination replaces conformal ALD with selective ALD, eliminating a high-resistivity barrier at the via interface. The solution also includes copper reflow technology that enables void free gap fill in narrow features. Electrical resistance at the via contact interface is reduced by up to 50 percent, improving chip performance and power consumption, and enabling logic scaling to continue to 3nm and beyond. An animation of the process sequence can be viewed at this link: https://bit.ly/3g8HMe1.

"A smartphone chip has tens of billions of copper interconnects, and wiring already consumes a third of the chip's power," said Prabu Raja, Senior Vice President and General Manager of the Semiconductor Products Group at Applied Materials. "Integrating multiple process technologies in vacuum allows us to reengineer materials and structures so that consumers can have more capable devices and longer battery life. This unique, integrated solution is designed to accelerate the performance, power and area-cost roadmaps of our customers."

The Endura Copper Barrier Seed IMS system is now being used by leading foundry-logic customers worldwide. Additional information about the system and other innovations for logic scaling will be discussed at Applied's 2021 Logic Master Class being held today.

About Applied Materials
Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible a better future. Learn more at www.appliedmaterials.com.

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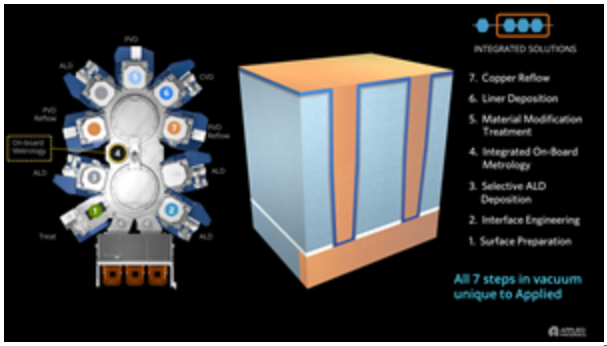
A photo accompanying this announcement is available at https://www.globenewswire.com/NewsRoom/AttachmentNg/5808956d-a82a-45d4-bb07-6e4804678159

Applied Materials' Endura® Copper Barrier Seed IMS™ System



Applied Materials' new Endura® Copper Barrier Seed IMS™ combines seven different process technologies in one system under high vacuum to improve chip performance and power consumption. An animation of the process sequence can be viewed here: https://bit.ly/3g8HMe1.

Source: Applied Materials, Inc.