Applied Materials Introduces New Systems to Accelerate DRAM and Advanced Packaging for AI Chips

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- *Innovations spanning DRAM and advanced packaging enable the 3D architectures behind cutting-edge AI chips*
- *A new epitaxy system optimized for DRAM fabs adds a critical logic-class step—boosting memory speed and efficiency while maximizing output within tight fab footprint and supply constraints*
- *New CMP and deposition systems target the most critical advanced packaging steps, delivering higher-yield chip stacking for HBM and logic*
- *New eBeam systems bring wafer-fab-grade metrology and defect review to advanced packaging, optimized to handle the unique challenges these packages present*

SANTA CLARA, Calif., June 25, 2026 (GLOBE NEWSWIRE) -- Applied Materials, Inc., the leader in materials engineering for the semiconductor industry, today introduced a suite of new chipmaking systems for building the advanced 3D chip architectures that power next-generation AI.

AI compute is increasingly constrained by memory, as model scale and data movement demands outpace gains in bandwidth, capacity and energy efficiency. This growing “memory wall” is accelerating adoption of advanced packaging architectures, including high bandwidth memory (HBM) and 3D stacking. These technologies deliver step-change improvements in bandwidth and efficiency but introduce new challenges in process complexity. Applied is enabling this transition with a materials engineering portfolio spanning DRAM, advanced packaging and process control, extending its leadership across each domain to help customers bring a new generation of AI chips to production faster and at higher yield.

Enhanced Epitaxy Brings Logic-Class Technology to Next-Generation DRAM

Epitaxy has been used for years in leading-edge logic, where precision growth of a crystalline material in the transistor channel has boosted performance well beyond what geometric scaling alone can deliver. Those same techniques are now becoming critical in DRAM peripheral transistors. Applied pioneered silicon germanium epitaxy in transistor channels more than a decade ago with its Centura™ Prime™ Epi system.

Enhanced Centura™ Prime™ Epi
Applied is now introducing an enhanced Centura™ Prime™ Epi system that selectively grows doped silicon germanium and silicon phosphorous in source/drain regions, combining advanced strain engineering with precise doping control. The result is higher drive current and transistor efficiency, enabling faster, more power-efficient DRAM operation—essential for the bandwidth demands of HBM and next-generation DDR. The new system also features a 20% smaller footprint, enabling higher tool density and faster capacity scaling in DRAM fabs.

“The transistor and materials technologies that drove performance gains in leading-edge logic are now becoming essential in DRAM,” said Dr. Prabu Raja, President of the Semiconductor Products Group at Applied Materials. “As DRAM scales to meet the bandwidth demands of HBM and AI workloads, the distinction between logic and memory process technology is converging. By leveraging our epitaxy leadership in leading-edge logic, Applied is uniquely positioned to drive this transition in DRAM.”

New CMP and Deposition Systems Target the Most Critical Advanced Packaging Steps

In recent years, advanced packaging has become as strategically important to the computing industry as on-chip transistor scaling. Modern AI server chips pack trillions of transistors by integrating multiple dies into a single package. HBM is a leading example of this approach, stacking DRAM chips on top of one another and connecting them with through-silicon vias (TSVs). Applied is the leader in process equipment for advanced packaging, including systems covering the majority of materials engineering steps required to create the TSVs, copper pillars and microbumps that connect stacked dies. Today, Applied is introducing three new systems targeting the most critical advanced packaging process steps.

Opta™ Quad CMP
Leveraging Applied’s leadership position in chemical mechanical planarization (CMP), the Opta™ Quad platform is engineered specifically for advanced packaging, where thicker films, longer polish times and tighter tolerances raise the risk of non-uniformity and yield loss. Opta Quad continuously monitors wafer conditions during polish and dynamically adjusts in real time, improving within-wafer uniformity and total thickness variation control. This is particularly critical for hybrid bonding—an emerging 3D stacking technology in which copper wiring and surrounding dielectrics from two chips are fused together in a single step, requiring near-perfect surface planarity for high-yield results.

Nokota™ VMax™ 2 ECD
As 3D stacks scale, uneven interconnects can leave gaps that prevent reliable contact between layers. Ensuring the TSVs and microbumps are leveled across the entire wafer becomes critical to stacking yield. Nokota™ VMax™ is an electrochemical deposition (ECD) system engineered for high-precision copper plating across a broad range of applications for next-generation packaging, from TSV fill for 3D stacking to fine-pitch interconnects such as microbump formation. Nokota VMax 2 introduces Adaptive Pattern Tuning (APT), which dynamically shapes the electric field to correct for layout-driven variation and improve plating uniformity across the wafer.

Producer™ Avila™ 2 PECVD
To fit more layers into a stack, HBM dies are thinned to roughly 1/25th the thickness of a standard wafer, making them prone to warpage and

deformation. These effects compound as layers are added, increasing the risk of bonding failure and yield loss. Producer™ Avila™ is a plasma-enhanced chemical vapor deposition (PECVD) system that improves the mechanical stability of ultra-thin DRAM dies by depositing stress-balanced dielectric films around TSVs, enabling reliable stacking of 12, 16, and future high-layer-count HBM designs. In addition to HBM, the system supports a range of advanced memory and logic integration schemes.

"Advanced packaging has become a primary driver of system-level performance, and the complexity of next-generation 3D architectures demands new levels of precision across every process step," Raja said. "Applied's leadership in dielectric CVD, ECD and CMP—combined with deep process integration expertise—gives customers the tools they need to scale 3D stacks reliably and at yield."

New eBeam Systems Bring Wafer-Fab Process Control to Advanced Packaging

Advanced packaging fabs are encountering defect and metrology challenges once exclusively found in wafer fabs. Feature dimensions have shrunk below the resolution limit of optical inspection tools, and particles that were tolerable with larger bumps now impact yield. A single defect can require scrapping an entire HBM stack, elevating process control to a strategic priority. Applied is extending its eBeam leadership with two new systems specifically designed for advanced packaging—both engineered to handle a wide range of substrate geometries and materials.

VeritySEM™ 7AP CD Metrology
The latest in Applied's VeritySEM™ portfolio for critical dimension (CD) metrology, VeritySEM™ 7AP enables precise measurement of features on thick, heterogeneous, and highly warped substrates common in HBM and chiplet architectures. VeritySEM AP systems automatically reconfigure to support a range of sizes and materials, while delivering sub-10nm sensitivity—orders of magnitude better than optical tools.

SEMVision™ G7AP Defect Analysis
SEMVision™ is the industry's leading eBeam defect analysis platform. SEMVision™ G7AP extends Applied's leadership into advanced packaging, enabling high-resolution defect review and automated classification across silicon, organic, and glass substrates. The system can accelerate yield learning by helping customers quickly distinguish critical defects from nuisance signals. SEMVision G7AP is already in production at leading memory and logic manufacturers supporting high-volume advanced packaging.

"Applied has been at the forefront of eBeam technology for decades," said Keith Wells, Group Vice President and General Manager of the Imaging and Process Control Group at Applied Materials. "As advanced packaging geometries scale below the resolution limit of optical tools, packaging fabs need eBeam-grade precision to both redetect and classify the defects. In developing the VeritySEM 7AP and SEMVision G7AP tools, Applied is transferring proven wafer fab expertise into packaging—purpose-built for the substrates and defect challenges of 3D architectures."

A media kit with additional information on the new systems is available on the Applied Materials website. Further details about Applied's advanced technologies will be provided at the company's DRAM and Advanced Packaging Master Class being held later today.

About Applied Materials
Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions that are at the foundation of virtually every new semiconductor and advanced display in the world. The technology we create is essential to advancing AI and accelerating the commercialization of next-generation chips. At Applied, we push the boundaries of science and engineering to deliver material innovation that changes the world. Learn more at www.appliedmaterials.com.

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