Forward-Looking Statements and Other Information

Today's presentations contain forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our investment and growth strategies, our development of new products and technologies, our business outlook for fiscal 2021 and beyond, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic and industry conditions; the effects of regional or global health epidemics, including the severity and duration of the ongoing COVID-19 pandemic; global trade issues and changes in trade and export license policies, including the recent rules and interpretations promulgated by the U.S. Department of Commerce expanding export license requirements for certain products sold to certain entities in China; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; acquisitions, investments and divestitures; changes in income tax laws; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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2021 Master Classes
WELCOME

Michael Sullivan
CVP, Head of Investor Relations

MEMORY MASTER CLASS | May 5, 2021
UPCOMING INVESTOR EVENTS

MASTER CLASSES

- Specialty semiconductors
- Heterogeneous design and advanced packaging
- Inspection and process control
AGENDA

9:00  PART 1  HOST: Mike Sullivan
Memory Thesis
Fireside Chat | Ed Doller

9:15  PART 2  HOST: Kevin Moraes, Ph.D.
Memory Technology
DRAM | Sony Varghese, Ph.D.
NAND | Sean Kang, Ph.D.

9:50  PART 3  HOST: Raman Achutharaman, Ph.D.
Memory Growth Opportunities

10:00 Q&A  Raman, Kevin, Mike
Historical WFE

- **1990 – 2000**: Equipment industry grows with Semi
- **2000 – 2013**: No growth cyclical / transition to 300mm
- **2013 – 2020**: Equipment industry grows with Semi

Source: Gartner, VLSI, Applied Materials.
Rising WFE Driven by New Devices and Applications

2000

PC + Internet

2010

Mobile + Social Media

2016

Artificial Intelligence + Visual Computing

- Internet of Things
- Machine Learning
- Autonomous Vehicles
- Big Data
- AR / VR

Av. WFE = $25.5B*
\[ \sigma = 8.0B \]

Av. WFE = $32.4B**
\[ \sigma = 3.0B \]

MEMORY DEMAND: CONTEXT

Big Data and Artificial Intelligence can transform entire industries – happening faster than many people think

Explosion of data storage requirements created by IoT, Big Data, AI and streaming video has only just begun

Data generation from new categories can potentially dwarf existing applications within a few years
Data Generation to Memory Relationship | Historical

**DRAM**

- $y = 0.0081x^{1.3065}$
- $R^2 = 0.9563$

**NAND**

- $y = 0.0022x^{2.0399}$
- $R^2 = 0.9569$

Incremental Data Generation (EB) vs. DRAM Shipments (EB) & NAND Shipments (EB)

Source: Cisco, VNI, Cisco, Gartner, Factset, Applied Materials internal analysis.

2008 to 2016 data from Cisco and Gartner, 2017 to 2020 projections from Cisco for data generation (VNI/ IP traffic), and industry average estimates for DRAM and NAND content shipments.
SEMI GROWTH NO LONGER LIMITED BY HUMAN CONSUMPTION

Data Generation By Category (ZB)

Source: Applied Materials

Applied Materials External Use
<table>
<thead>
<tr>
<th>Semi content per unit</th>
<th>2015</th>
<th>2020</th>
<th>2025F</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH END SMARTPHONE</td>
<td>$100</td>
<td>$170</td>
<td>$275</td>
</tr>
<tr>
<td>AUTO (GLOBAL AVERAGE)</td>
<td>$310</td>
<td>$460</td>
<td>$690</td>
</tr>
<tr>
<td>DATACENTER SERVER (CPU + ACCELERATOR)</td>
<td>$1,620</td>
<td>$2,810</td>
<td>$5,600</td>
</tr>
<tr>
<td>SMARTHOME (GLOBAL AVERAGE)</td>
<td>$2</td>
<td>$4</td>
<td>$9</td>
</tr>
</tbody>
</table>

SILICON CONTENT GROWING AS EVERYTHING GETS SMARTER

Source: Applied Materials
Historical WFE Mix

- Foundry / Logic > 55%
- Memory < 45%

Long-Term Average

Foundry / Logic vs. Memory mix consistent over time:

- 10-year and 20-year averages: Foundry / Logic > 55%
- Foundry / Logic > Memory in 17 of past 20 years

Source: Gartner, VLSI, Applied Materials
# Memory Market Segmentation

<table>
<thead>
<tr>
<th></th>
<th>ACCESS TIME</th>
<th>GB COST ($)*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VOLATILE</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SRAM</td>
<td>Nanoseconds</td>
<td>&gt;$1,200</td>
</tr>
<tr>
<td>DRAM</td>
<td>~35 nanoseconds</td>
<td>~$5.25</td>
</tr>
<tr>
<td><strong>PERSISTENT</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MRAM</td>
<td>~50 nanoseconds</td>
<td>&gt;$1,800</td>
</tr>
<tr>
<td>PCRAM</td>
<td>&gt;100 nanoseconds</td>
<td>~$2.85</td>
</tr>
<tr>
<td>NAND SSD</td>
<td>~100 microseconds</td>
<td>~$0.15</td>
</tr>
<tr>
<td>Hard Disk Drive</td>
<td>~3 milliseconds</td>
<td>~$0.02</td>
</tr>
</tbody>
</table>

* Cost estimates based on retail devices and pricing

**Today’s Focus**

- **SPEED & RELIABILITY**
- **COST**
PART 2
Memory Challenges and Roadmaps – DRAM

Sony Varghese, Ph.D.
Director, Strategic Marketing

MEMORY MASTER CLASS | May 5, 2021
DRAM: High-Speed Volatile Memory

- Die density - 16Gb
- Package density – 512GB
- Speed – 7200Mbps

3 key PPACt enablers – Cell, Peri, and Package

Cross-section of DRAM chip

Source: TechInsights
Peri transistor variability ($V_t$ mismatch) impacts sensing margin

Sensing margin is shrinking with decreasing capacitor charge

Gate length scaling lagging projection for acceptable sensing margin

Source 1: A. Spessot, IEEE Transactions on electron devices, vol. 67, no. 4, April 2020
Source 2: TechInsights and Applied Materials projections
# DRAM Scaling Roadmap

<table>
<thead>
<tr>
<th>Year of first production</th>
<th>Node (nm)</th>
<th>Cell capacitance (fF)</th>
<th>Periphery gate length (nm)</th>
<th>Key inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>2017</td>
<td>20</td>
<td>13</td>
<td>100-115</td>
<td>Lattice for capacitor</td>
</tr>
<tr>
<td>2019 ~</td>
<td>17</td>
<td>10</td>
<td>75-90</td>
<td>SAQP&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td>2021 ~</td>
<td>15</td>
<td>7</td>
<td>65-80</td>
<td>DDR5, More SAQP, EUV, HKMG&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>2023 ~</td>
<td>13</td>
<td>5</td>
<td>50-60</td>
<td>Commodity DRAM HKMG&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>2025 ~</td>
<td>11</td>
<td>3</td>
<td>45-55</td>
<td>Low resistance metal</td>
</tr>
<tr>
<td>2025 +</td>
<td>3D DRAM</td>
<td>4+</td>
<td>New CMOS</td>
<td>Layered high mobility channel&lt;sup&gt;3&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

---

**Samsung Announces Industry’s First EUV DRAM with Shipment of First Million Modules**

- **Korea on March 25, 2020**
- [View Details](#)

**Micron: 1α Process Technology to Improve DRAM Density By Up to 40%**

- **By Anton Shilov January 26, 2021**
- Micron announces impressive 1α fabrication process for DRAM.

**SK hynix Launches World’s First DDR5 DRAM**

- **October 6, 2020**
- [View Details](#)

**Samsung Develops Industry’s First HKMG-Based DDR5 Memory: Ideal for Bandwidth-Intensive Advanced Computing Applications**

- **Korea on March 25, 2021**
- [View Details](#)

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<sup>1</sup> SAQP – Self Aligned Quadruple Patterning

<sup>2</sup> HKMG – High k Metal Gate

<sup>3</sup> 1X higher mobility than 3DNAND Channel

Applied Materials External Use
# Levers for DRAM Scaling

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Key modules</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell</td>
<td>Capacitor, Active silicon area, Word line / bit line</td>
<td><img src="cell_current.png" alt="Diagram" /></td>
<td><img src="cell_inflections.png" alt="Diagram" /></td>
</tr>
<tr>
<td>Periphery</td>
<td>Interconnect, Transistor</td>
<td><img src="periphery_current.png" alt="Diagram" /></td>
<td><img src="periphery_inflections.png" alt="Diagram" /></td>
</tr>
<tr>
<td>3D stacking</td>
<td>Bond pad, Thru silicon via (TSV), Bump</td>
<td><img src="3d_current.png" alt="Diagram" /></td>
<td><img src="3d_inflections.png" alt="Diagram" /></td>
</tr>
<tr>
<td>New architecture</td>
<td>High mobility channel, Conductor etch, Selective removal, HAR gapfill, Advanced doping</td>
<td><img src="architecture_current.png" alt="Diagram" /></td>
<td><img src="architecture_inflections.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>
# Levers for DRAM Scaling: Cell Region

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell region</td>
<td><img src="image1.png" alt="Capacitor" /> <img src="image2.png" alt="Active area" /></td>
<td><img src="image3.png" alt="Thinner capacitor" /> <img src="image4.png" alt="Shrinking active area" /></td>
</tr>
</tbody>
</table>

## Module

<table>
<thead>
<tr>
<th>Module</th>
<th>High Value Problems</th>
<th>Solutions</th>
</tr>
</thead>
</table>
| Capacitor     | High aspect ratio capacitor fabrication  
Higher etch profile variability and defects                                      | New hardmask materials  
Co-optimized etch technology with metrology feedback                                       |
| Active silicon area | Shrinking Si active area  
Reduced drive current and increased variability                               | Patterning SAQP or EUV with HAR Etch  
Low Si loss from oxidation, Low damage from implant                                         |
DRAM Capacitor Scaling Challenges

- Shrink + geometry change = High AR
- Need taller mask for patterning
- Higher etch variability and defects

- Double-sided vs. single-sided
- Cell size 10\(^{-4}\) \(\mu\)m\(^2\)
- Capacitor aspect ratio
  - 30 2x 2y 1x 1y 1z 1a 1b 1c 1d

- Nitride affects circularity of mold profile
- Varying hole sizes in hard mask

Local CD variation:
- Unopened holes
- Bridging / shorts
Innovations to Enable Low Variability High AR Etch Process

Draco™: New hard mask material (Higher modulus and selectivity)

New high temp etch technology (Better profile and CD uniformity)

Unique metrology (Faster and better sampling error)

- Tunable film properties for selectivity
- Unique precursor chemistry

- Industry leading >200°C capability
- Higher conductance Sym3® design

- Non-destructive, bottom imaging with actionable measurements

* CD = Critical Dimension
Variability and Defect Reduction with Co-Optimization

Thinner mask with lower AR + New etch

- Local CD uniformity improved
- Bridging defects substantially reduced

Enabling improved CD uniformity and defect performance

- Local CD uniformity improved by 50%
- Bridging defects reduced by 100X

AR = Aspect Ratio
CD = Critical Dimension
# Levers for DRAM Scaling: Periphery Region

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Periphery</td>
<td>TEOS dielectric Cu Poly / SiON</td>
<td>Low-k + Adv CuBS HKMG</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module</th>
<th>High Value Problems</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor</td>
<td>( V_t ) variability High gate leakage current</td>
<td>New materials (Metal Gate, Dipole) Interface engineering (High-k, Inter Layer, Channel)</td>
</tr>
<tr>
<td>Interconnect</td>
<td>Power loss and RC delays with narrow pitch Early device failure from electromigration</td>
<td>Low capacitance dielectric Advanced copper interconnect</td>
</tr>
</tbody>
</table>
PPACt Scaling of DRAM Peri Transistors with HKMG

**HIGH VALUE PROBLEM**

Thinner insulation layer = higher leakage

![Chart showing leakage current density vs. EOT](chart.png)

**PPACt gains with HKMG**

- **13%** lower power
- **2X** speed

Source: Samsung newsroom, Mar 25, 2021

**REQUIREMENTS**

- Multiple new materials
- 6-7 materials stack
- High complexity

**APPLIED LEADERSHIP PRODUCTS**

- Metal gate
- Dipole for Vt engineering
- PMOS channel

- High-k film treatments
- Interlayer/HK interface
- Interlayer Engineering
- Channel interface

**APPLIED LEADERSHIP**

**PRODUCTS**

Accelerating adoption of Logic-like process innovations in DRAM
DRAM Periphery: Interconnect Scaling

**HIGH VALUE PROBLEM**

Periphery scaling reduces wire pitch ($w_d$) and copper line widths ($w_m$).

At reduced pitch, signal delay and power losses increase

$$RC\text{ Delay} = \rho k \varepsilon_0 \frac{L^2}{w_m w_d}$$

$$\text{Power} = CV^2 F$$

Higher current density in narrow lines, cause early electromigration failures

- $\rho$: Conductor Resistivity
- $k$: Effective Dielectric Constant (Low $k$)
- $\varepsilon_0$: Permittivity in Vacuum
- $L$: Interconnect Length
- $w_m$: Metal Width
- $w_d$: Metal Spacing
- $C$: Capacitance
- $V$: Voltage
- $F$: Frequency

Source: Applied Materials
DRAM Adopting Interconnect Innovations from Logic

**Technology solutions**

<table>
<thead>
<tr>
<th>Dielectric constant</th>
<th>TEOS</th>
<th>Low-k</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;4.0</td>
<td>2.9-3.0</td>
<td>&gt;25%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Electromigration lifetime</th>
<th>Dielectric</th>
<th>Co Metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;10x</td>
<td>Co Metal</td>
<td>Dielectric</td>
</tr>
</tbody>
</table>

**Adoption of low-k**

TEOS silicon oxide → low-k

**Adoption of Cobalt capping**

Cu interconnect + Co capping

**Industry leading interconnect technology**

Producer® Black Diamond®

Industry leading low-k material

Endura® CuBS + CVD Cobalt

Industry leading interconnect technology
### Levers for DRAM Scaling: New Architecture

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Today</th>
<th>Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>New architecture</td>
<td><img src="image" alt="Planar DRAM" /></td>
<td><img src="image" alt="3D DRAM" /></td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="Capacitor" /></td>
<td><img src="image" alt="Word line" /></td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="Transistor" /></td>
<td><img src="image" alt="Capacitor" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module</th>
<th>High Value Problems</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D DRAM</td>
<td>Patterning costs challenges, Inadequate sensing margin</td>
<td>High mobility channel EPI /PVD/ALD, Conductor etch, HAR gap fill, Selective removal, Advanced doping</td>
</tr>
</tbody>
</table>
Planar DRAM Scaling Limitations

- In production Capacitor charge 7fF
- Projected Capacitor charge 3fF
  - Array Si 12nm x 220nm
- SAQP Limit

Industry targets 20% density increase per node

SAQP limit beyond n+4

Cost challenges from patterning may make scaling uneconomical

Reduction in capacitor charge → inadequate sensing margin

New methods to scale are needed to meet PPAC
Will 3D DRAM be Fabricated Like 3D NAND?

Can DRAM scale by stacking 1 cell over the other? It worked for NAND

DRAM must operate 1000X faster than NAND
Requirements more similar to logic Gate-All-Around (GAA)

<table>
<thead>
<tr>
<th></th>
<th>NAND cell</th>
<th>DRAM cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write speed</td>
<td>50,000 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>Endurance</td>
<td>1e4 cycles</td>
<td>1e18 cycles</td>
</tr>
<tr>
<td>Channel mobility</td>
<td>Low (poly Si)</td>
<td>High (Si)</td>
</tr>
<tr>
<td>Storage discharge</td>
<td>Slow (charge trap)</td>
<td>Quick (capacitor)</td>
</tr>
</tbody>
</table>

New material innovations required to enable higher mobility, ultra-low defect channels for 3D DRAM
Enabling the Roadmap to 3D DRAM PPACt Scaling

Unit
Process
Leadership

High mobility channel
Epi /PVD/ALD
Conductor etch
HAR gapfill
Selective removal
Advanced doping

Integrated Materials Solutions Leadership
# Enabling PPACt Roadmap for DRAM

<table>
<thead>
<tr>
<th></th>
<th>DDR4, 1.2V</th>
<th>DDR5, 1.1V</th>
<th>DDR6</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>2.3Gbps 8Gb</td>
<td>3.2Gbps 8Gb</td>
<td>7.2Gbps 16Gb 16/32Gb</td>
</tr>
<tr>
<td>2017</td>
<td>2.6Gbps 8Gb</td>
<td>4.8Gbps 16Gb</td>
<td>12Gbps* 32Gb</td>
</tr>
<tr>
<td>2019</td>
<td>3.2Gbps 8Gb</td>
<td>5.6Gbps 16Gb</td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td>4.8Gbps 16Gb</td>
<td>7.2Gbps 16Gb</td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td>5.6Gbps 16Gb</td>
<td>7.2Gbps 16/32Gb</td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td>7.2Gbps 16Gb</td>
<td>7.2Gbps 16/32Gb</td>
<td></td>
</tr>
<tr>
<td>2021</td>
<td>8Gb</td>
<td>16Gb</td>
<td></td>
</tr>
<tr>
<td>2021</td>
<td>8Gb</td>
<td>16Gb</td>
<td></td>
</tr>
<tr>
<td>2023</td>
<td>12Gbps* 32Gb</td>
<td>12Gbps* 32Gb</td>
<td></td>
</tr>
<tr>
<td>2023</td>
<td>12Gbps* 32Gb</td>
<td>12Gbps* 32Gb</td>
<td></td>
</tr>
<tr>
<td>2025</td>
<td>3D DRAM</td>
<td>3D DRAM</td>
<td>3D DRAM</td>
</tr>
</tbody>
</table>

- **SAQP**
- **Low Damage Implant**
- **HKMG**
- **EUV**
- **Low K**
- **Capacitor Hardmask**
- **Co Capping**
- **Low R Metals**

Well positioned with leadership products and integrated materials solutions
PART 2
Memory Challenges and Roadmaps – 3D NAND

Sean Kang, Ph.D.
Sr. Director

MEMORY MASTER CLASS | May 5, 2021
3D NAND: A High-Density Storage Memory

State of the art technology:
- Die density: 1Tb
- Number of layers: 176 pairs
- Maximum IO speed: 1.6 Gbps
- Bit/cell: QLC
Physics of 3D NAND and Implications for Scaling

How 3D NAND works

Write
- Drain: 0V
- Gate: 20V
- Source: 0V

Erase
- Gate: 0V

Read
- 1V
- Gate: Vr1

Bits Scaling

1bit - SLC
- (a) SLC
- VR
- VT

2bit - MLC
- (b) MLC
- VR1 VR2 VR3
- VR
- VT

3bit - TLC
- (c) TLC
- VR1 VR2 VR3
- VR
- VT

Vol. 105, No. 9, September 2017 | Proceedings of the IEEE 1609
### 3D NAND Scaling Roadmap

<table>
<thead>
<tr>
<th>Year of first production</th>
<th>Node (pair)</th>
<th>Stack height (µm)</th>
<th>Pair thickness (nm)</th>
<th>Key structure inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>~30</td>
<td>~2.5</td>
<td>~70</td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td>~70</td>
<td>~5</td>
<td>~60</td>
<td></td>
</tr>
<tr>
<td>2019 ~</td>
<td>&gt;100</td>
<td>~7</td>
<td>~50</td>
<td>Staircase Opt.¹</td>
</tr>
<tr>
<td>2021 ~</td>
<td>&gt;150</td>
<td>~8.5</td>
<td>45 ~ 50</td>
<td>2 Tier, CuA²</td>
</tr>
<tr>
<td>2023 ~</td>
<td>&gt;250</td>
<td>&gt;10</td>
<td>40 ~ 45</td>
<td>Cell Design³</td>
</tr>
<tr>
<td>2025 ~</td>
<td>&gt;350</td>
<td>&gt;&gt; 10</td>
<td>~40</td>
<td>&gt;2 Tier, CoA⁴</td>
</tr>
</tbody>
</table>

---

1. Staircase optimization for area saving
2. CuA: CMOS Under Array
3. Cell layout intensification
4. CoA: CMOS over Array

---

*Samsung plans to 'double-stack' 3D-NAND flash memory*

*SK hynix Unveils the Industry's Most Multilayered 176-Layer 4D NAND Flash*

*Intel’s New Optane And 144-Layer NAND SSDs Enable PCs As Well As Data Centers*

*YTMC stakes claim for top table with 128 layer 1.33Tb QLC 3D NAND*

*November 9, 2020 at 4:01 PM EST
Micron Ships World's First 176-Layer NAND, Delivering A Breakthrough in Flash Memory Performance and Density*

*Kioxia and Western Digital build 162-layer 3D NAND*

*Dec 15, 2020, 8:36 AM EST
Kioxia first to enter the 162-layer 3D NAND market*
# Three Levers for 3D NAND Scaling

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral</td>
<td>Staircase</td>
<td>CMOS near Array</td>
</tr>
<tr>
<td></td>
<td>Memory Holes</td>
<td>Slit</td>
</tr>
<tr>
<td>Vertical</td>
<td>~100p</td>
<td>&gt;100p</td>
</tr>
<tr>
<td></td>
<td>+ Pairs</td>
<td>- Pitch</td>
</tr>
<tr>
<td>Bits per cell</td>
<td>3b/c 8 states</td>
<td>4b/c 16 states</td>
</tr>
</tbody>
</table>
## Levers for 3D NAND Scaling: Lateral

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lateral</td>
<td>Staircase</td>
<td>CMOS near Array</td>
</tr>
<tr>
<td></td>
<td>Memory Holes</td>
<td>Slit</td>
</tr>
</tbody>
</table>

### High Value Problems

<table>
<thead>
<tr>
<th>Module</th>
<th>Problems</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Staircase</td>
<td>Single flight not scalable, Consumes 1-2% die</td>
<td>Zig-zag staircase architecture, Multi-pair etch and large HAR gap fill</td>
</tr>
<tr>
<td>CMOS</td>
<td>CMOS near array consumes 30% of die, CuA: Transistor higher thermal budget, CoA: W2W bonding</td>
<td>Architecture change, CuA or CoA, CuA: Optimized ion implant and annealing, CoA: Low dishing CMP and heterogeneous bonding</td>
</tr>
<tr>
<td>Memory array</td>
<td>Memory hole density, Slits consume &gt;10% of array (holes + slits)</td>
<td>SiN exhume and ALD</td>
</tr>
</tbody>
</table>
3D NAND Staircase Area Savings

Limitations
- Traditional staircase has area penalty, not scalable to more pairs

New Capabilities
- Zig-zag Staircase brings new challenges in profile control, CD/ER uniformity, throughput and cost

Adoption
- 3 in production, others in R&D

Cross-section Images from TechInsights
CD: Critical Dimension
ER: Etch Rate

Traditional Staircase – Single Flight
- 48 Pairs
- ~60 μm long
- ~90% Staircase Area Savings

Zig-zag Staircase – Multiple Flights
- 96 Pairs
- ~10 μm long

Continuing leadership position with Sym3 etch
3D NAND CMOS Area Savings

Today’s CMOS and array are side by side

Under (CuA)  
Over (CoA)

Cell – Memory array area  
Peri – Peripheral logic CMOS area

<table>
<thead>
<tr>
<th>Benefit</th>
<th>Relative low cost</th>
<th>Higher CMOS performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Challenges</td>
<td>Fabrication thermal budget</td>
<td>Wafer to wafer bonding</td>
</tr>
<tr>
<td>New capability required</td>
<td>Specialized implant &amp; thermal Less stress metal fill</td>
<td>More copper interconnects CMP and Die to wafer bonding</td>
</tr>
<tr>
<td>Adoption</td>
<td>3 customers</td>
<td>1 customer</td>
</tr>
</tbody>
</table>
New Process Steps Enable CuA and CoA

**Impact to transistor technology**

- Standard source/drain without LE and co-implants
- CuA requires low energy with co-implants

**Impact to interconnect technology**

<table>
<thead>
<tr>
<th>Material</th>
<th>Conventional</th>
<th>CoA</th>
<th>CuA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tungsten</td>
<td>2</td>
<td>1-2</td>
<td>4</td>
</tr>
<tr>
<td>Copper</td>
<td>1</td>
<td>4-5</td>
<td>1</td>
</tr>
<tr>
<td>Aluminum</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Packaging</td>
<td>-</td>
<td>W2W</td>
<td>-</td>
</tr>
</tbody>
</table>

**Notes:**
- CMOS peri wafer
- Memory array wafer
- Bond line
- High thermal budget CMOS processing
- Deep junction
- Shallow junction depth
- Gate-SDE overlap
Hybrid Bonding | Enabling Novel CoA NAND Architecture

W2W hybrid bonded (CoA)

Key challenges

1. Bulk Cu removal
2. Barrier removal
3. Topography correction

Barrier / Seed PVD → Cu pad fill ECD → CMP with tuned dishing control

Reflexion® LK Cu CMP
Process optimized over 3 platens

1. Bulk Cu removal
2. Barrier removal
3. Topography correction

Dishing Range

POR Reflexion LK

>60% improvement

Target

PVD: Physical Vapor Deposition
ECD: Electro-Chemical Deposition
CMP: Chemical Mechanical Polishing
WiW: Within Wafer
POR: Process of Record
## Levers for 3D NAND Scaling: Vertical

<table>
<thead>
<tr>
<th>Scaling lever</th>
<th>Current</th>
<th>Inflections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vertical</td>
<td>~100p</td>
<td>&gt;100p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;120p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt;150p</td>
</tr>
<tr>
<td></td>
<td>+ Pairs</td>
<td>- Pitch</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+ Tiers</td>
</tr>
</tbody>
</table>

### Module High Value Problems Solutions

<table>
<thead>
<tr>
<th>Module</th>
<th>High Value Problems</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ Pairs</td>
<td>Hardmask selectivity and etch cost</td>
<td>New Hardmask required</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Etch cost effectiveness decreases with AR</td>
</tr>
<tr>
<td>- Pitch</td>
<td>Removal of SiN and metal fill Pattern collapse</td>
<td>SiN Exhume and ALD Metal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High modulus ON</td>
</tr>
<tr>
<td>+ Tiers</td>
<td>Complex process, e.g. staircase integration Higher aspect ratio structure</td>
<td>New hardmask and Etch</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ALD and CVD Fill</td>
</tr>
</tbody>
</table>
Co-Optimized Hardmask Deposition and Etch

HIGH VALUE PROBLEM

Increasing hardmask thickness

Co-optimized hardmask etch

More selective hardmask

Carbon hardmask

Selective hardmask

High selectivity
Low stress
Transparent film

Conventional etch

Advanced etch

Unique source design
Improved profile
Available strip solution

In high volume production for multiple layers

Source: Applied Materials
High Aspect Ratio Large Area Gapfill

HIGH VALUE PROBLEM

- Large gaps to fill > 2um
- Aspect ratio > 10:1
- Impacted by shrinkage

Gapfill oxide

- Low shrinking film
- High deposition rate
- Tunable stress

Complete Fill Advanced CVD

In high volume production

Simplified planarization

- Excellent dishing performance
- Eliminates etchback step

Etchback + Buff CMP

- Direct CMP Only
  - Low Over-Burden

In high volume production

CMP: Chemical Mechanical Polishing
**3D NAND Vertical Scaling | Metal Gapfill**

**HIGH VALUE PROBLEM**

- **Conventional CVD W**
- **Seam suppressed CVD W**

Gapfill voids trap corrosive gas
Tungsten stress damages features

**Seam suppressed gapfill**

- Nucleation
- Treatment
- Bottom-up gapfill

**Low stress gapfill**

- Conventional CVD W
- Seam suppressed CVD W

- 3x improvement

**Step increase with CuA**

- Today
- CuA

- 2x increase

Source: Applied Materials

SSW – Seam suppressed tungsten
## Enabling PPACt Roadmap for NAND

<table>
<thead>
<tr>
<th>256Gb/512Gb</th>
<th>512Gb/1Tb</th>
<th>2Tb+</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TLC</strong></td>
<td><strong>TLC / QLC</strong></td>
<td><strong>QLC / QLC+</strong></td>
</tr>
<tr>
<td>~30L</td>
<td>&gt;100L</td>
<td>&gt;250L</td>
</tr>
<tr>
<td>~70L 1Gbps</td>
<td>&gt;150L 3Gbps</td>
<td>&gt;350L &gt;4Gbps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Year</th>
<th>Year</th>
<th>Year</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>2017</td>
<td>2019</td>
<td>2021</td>
</tr>
<tr>
<td>2023</td>
<td>2025</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **High AR hardmask dep/etch**
- **Seam suppressed W**
- **Optimized Junction CuA**
- **High selectivity hardmask dep/etch**
- **HAR gapfill, direct CMP**
- **Barrier-less metal**
- **Heterogeneous bonding CoA**

---

Well positioned with leadership products and integrated materials solutions
PART 3

Memory Growth Opportunities

Raman Achutharaman, Ph.D.
GVP, Head of Technology, Strategy, and Marketing

MEMORY MASTER CLASS | May 5, 2021
AGENDA

9:00   PART 1   HOST: Mike Sullivan
       Memory Thesis
       Fireside Chat | Ed Doller

9:15   PART 2   HOST: Kevin Moraes, Ph.D.
       Memory Technology
       DRAM | Sony Varghese, Ph.D.
       NAND | Sean Kang, Ph.D.

9:50   PART 3   HOST: Raman Achutharaman, Ph.D.
       Memory Growth Opportunities

10:00  Q&A     Raman, Kevin, Mike
Significant Momentum Across Device Types

Patterned growth + new products/solutions = Increased memory share, balanced portfolio

Source: Gartner, VLSI, Applied Materials
Unit process leadership and broadest portfolio
MATERIALS CREATION, MODIFICATION, REMOVAL, ANALYSIS

Unique combinations of technologies
CO-OPTIMIZATION INTEGRATED MATERIALS SOLUTIONS (IMS), PACKAGING

Actionable insight / time to market acceleration
ACTIONABLE INSIGHT ACCELERATOR (AI^x™)

Applied = PPACt Enablement Company
Going Beyond Unit Process Tools to Deliver Solutions

UNIT PROCESS LEADERSHIP
+ BROADEST PORTFOLIO

CO-OPTIMIZATION OF PROCESSES / TOOLS

INTEGRATED MATERIALS SOLUTIONS

FASTER TIME TO MARKET, HIGHER VALUE, STICKIER

SENSORS + eBeam + AI / ML

~40% of our products now co-optimized
~30% of our products now integrated

New
Applied AIx™ Actionable Insight Accelerator

**real-time ability to see into the process** with innovative sensors, in-vacuum metrology

+ **massive actionable data** with unique metrology

+ **AIx™ analytics platform** across all Applied tools

- ChamberAI™ ML algorithms
- AppliedPRO™
- Digital twin models
- Integrated controls

- >10,000 process possibilities per tool
- >1,000,000 possibilities per integrated flow

- 100X faster
- 50% higher resolution

Making every stage faster and better: R&D, ramp and HVM

2X faster with 30% better process window
Introducing Materials Engineering Solutions for DRAM Scaling

NEWS RELEASE

Applied Materials Introduces Materials Engineering Solutions for DRAM Scaling

- New Draco™ hard mask material co-optimized with Sym3® Y etcher to accelerate DRAM capacitor scaling
- DRAM makers adopting Black Diamond®, the low-k dielectric material pioneered by Applied Materials to overcome interconnect scaling challenges in logic
- High-k metal gate transistors now being introduced in advanced DRAM designs to boost performance and reduce power while shrinking the periphery logic to improve area and cost

SANTA CLARA, Calif., May 5, 2021 – Applied Materials, Inc. today announced materials engineering solutions that give its memory customers three new ways to further scale DRAM and accelerate improvements in chip performance, power, area, cost and time to market (PPACt).

The digital transformation of the global economy is generating record demand for DRAM. The Internet of Things is creating hundreds of billions of new computing devices at the edge which are driving an exponential increase in data transmitted to the cloud for processing. The industry urgently needs breakthroughs that can allow DRAM to scale to reduce area and cost while also operating at higher speeds and using less power.

Applied Materials is working with DRAM customers to commercialize three materials engineering solutions that create new ways to shrink as well as improve performance and power. The solutions target three areas of DRAM chips: storage capacitors, interconnect wiring and logic transistors. They are now ramping into high volume and are expected to significantly increase Applied’s DRAM revenue over the next several years.
Growing by Enabling the Capacitor Roadmap

$1B$ cumulative TAM opportunity

$>4X$ annual revenue growth

Year
FY’20
FY’24F

Breaking tradeoffs: area, capacitance, variability

Innovative technologies + acceleration with co-optimization + acceleration with metrology

Delivering node-over-node PPAC$t$ gains
$\uparrow$ performance, $\uparrow$ yield, $\downarrow$ area

DTOR / PTOR at major DRAM customers

DTOR = Development Tool of Record
PTOR = Production Tool of Record
Leadership in PPACt Solutions for Periphery Scaling

>$2B cumulative TAM opportunity

>3X annual revenue growth

Leadership products for HKMG transistors and interconnects

Decades of experience with logic-like processing

Delivering node-over-node PPACt gains ↓power, ↑performance, ↑yield, ↓area

DTOR / PTOR at major DRAM customers

Year

FY’20

FY’24F

DTOR = Development Tool of Record
PTOR = Production Tool of Record
Well Positioned for Growth in Packaging

Early innings of multi-year growth

- #1 in bond-pad, bump and TSV
- Broad product portfolio + full-flow lab
- Key eco-system partnerships
- Delivering system level PPACt gains
  - ↓ R, ↓ power, ↓ area, ↑ performance

FY'20 FY'24F

$500M

TSV = Through Silicon Via
TAKEAWAY
Messages

1. ‘AI era’ = **Secular growth** and accelerated innovation

2. Applied = The **PPACt enablement** company

3. **Uniquely positioned** to accelerate the PPACt roadmap
   Unit processes, unique combinations, actionable insight acceleration

4. Multiple big **inflections and growth opportunities** for Applied Materials

---

* Free cash flow = operating cash flow – net capital expenditures

** Non-GAAP adjusted EPS