MASTER CLASS June 25, 2026

Powering DRAM and Advanced Packaging Inflections

with Materials Innovation and Process Control

APPLIED MATERIALS

Forward Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including changes in interest rates and prices for goods and services; global trade issues, changes in trade and export regulations, license requirements, and their interpretation, and our ability to obtain licenses or authorizations on a timely basis, if at all; changes in tariffs, any retaliatory measures, and our ability to mitigate the impact of tariffs; the effects of geopolitical turmoil or conflicts; demand for semiconductor chips and electronic devices; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; cybersecurity incidents affecting us or our suppliers, customers or vendors; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our filings with the Securities and Exchange Commission, including our most recent Forms 10-K, 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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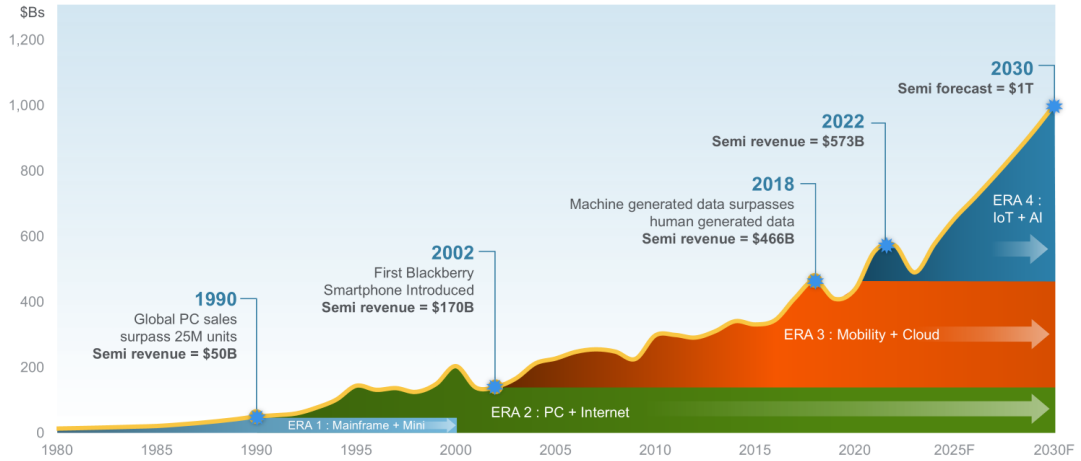
Michael Sullivan

Corporate Vice President
Head of Investor Relations

APPLIED MATERIALS

Prior View of Semi and WFE Markets

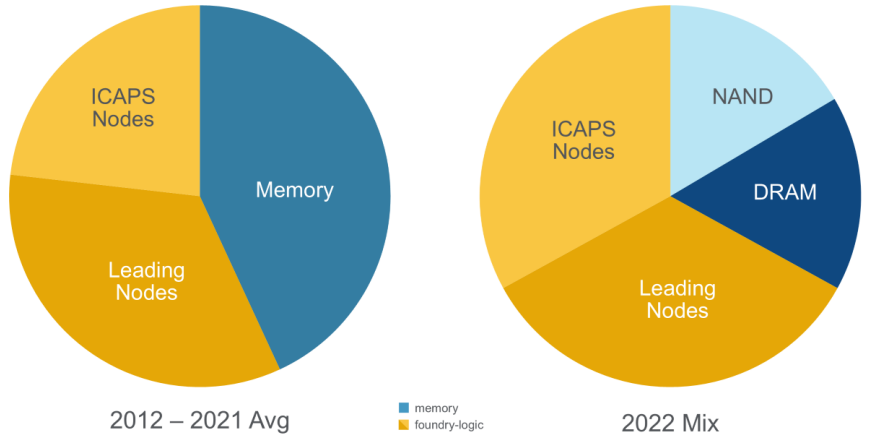
Our Semiconductor Industry Market Thesis



IoT + AI Era is the 4th and Biggest Age of Computing

Source 2030 forecast: TechInsights, McKinsey & Company, SEMI. Source Historical data: SIA, TechInsights, Applied Materials.

Expect Long-Term WFE to be Balanced: ICAPS, Leading, Memory



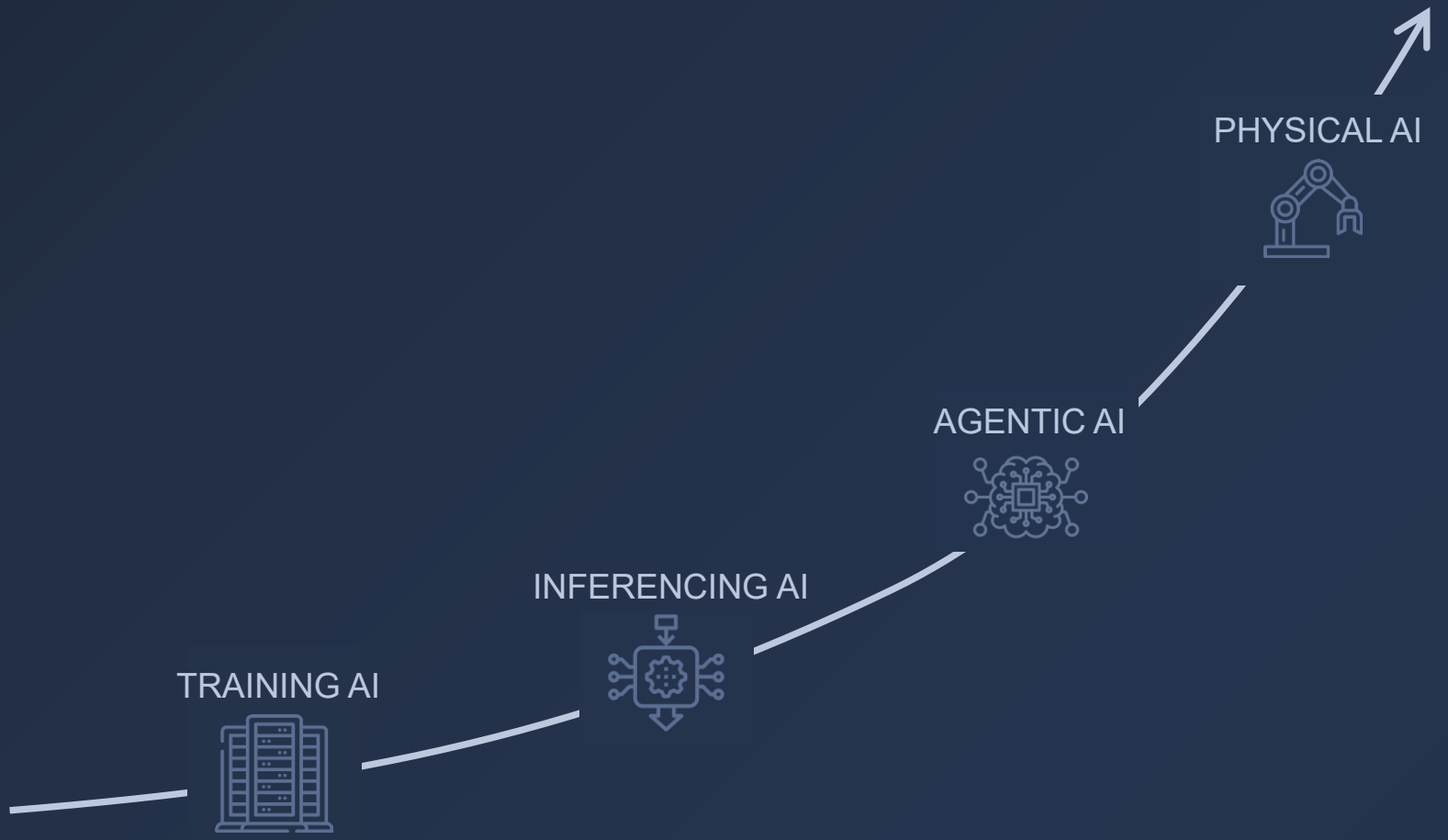
Long-term mix expected to be similar

Source: Gartner, TechInsights, Applied estimates. Leading nodes refers to 3nm, 5nm and 7nm.

APPLIED MATERIALS

AI Accelerating Semiconductor Demand

WAVES OF AI-DRIVEN GROWTH



Semiconductor industry revenues can potentially reach

$1T

this year

Source: SIA, Applied Materials

WFE Market Outlook

MOST ENABLING TECHNOLOGIES FOR AI COMPUTING PERFORMANCE AND POWER

DEVICE	INFLECTIONS
Leading-Edge Foundry/Logic	Gate-all-around transistors Backside power delivery
DRAM	$4F^2$ 3D DRAM
Advanced Packaging	High-bandwidth memory (HBM) Hybrid bonding Panel substrates
NAND	Increased layers, technology transitions
ICAPS	Compound semi (SiC, GaN) Photonics

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#1 Process Equipment Company in All Three Markets

ICAPS = IoT, Communications, Auto, Power, Sensors; represents nodes 10nm and larger

AGENDA

9:00	**Mike Sullivan** Welcome and Introduction **Kevin Moraes, Ph.D.** Innovation and Technology Strategy
9:15	**Sony Varghese, Ph.D.** DRAM and High Bandwidth Memory (HBM)
9:30	**Jinho An, Ph.D.** Advanced Packaging
9:45	**Lior Engel** Process Control
10:00	**Q&A** Kevin, Sony, Jinho, Lior, Mike

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Kevin Moraes, Ph.D.

Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

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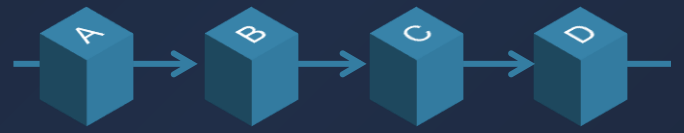
Inflection-Focused Innovation

Broad Capabilities Delivered as Unique Connected Solutions

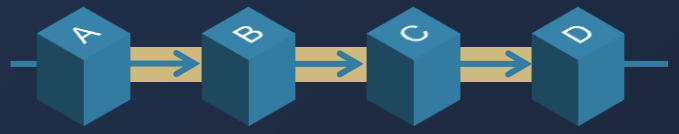
	Applied		Competitors			
ALD	✓	✓			✓	✓
Bonding	partner					✓
Cleans	partner				✓	✓
#1 CMP	✓					
#1 CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
#1 Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace	partner					✓
#1 Implant	✓					
Lithography	partner		✓			
M&I (optical)	✓			✓		
#1 M&I (eBeam)	✓		✓	✓		
#1 PVD	✓			✓		
#1 Thermal	✓					✓
Track						✓

UNIQUE COMBINATIONS

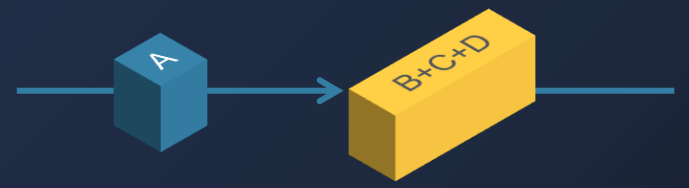
Unit Process Tools



Co-optimized Solutions



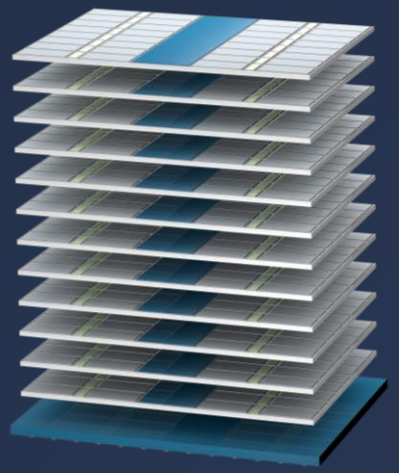
Integrated Materials Solutions (IMS™)



Applied Materials DRAM Share Growth

DRAM Leadership

increased share by ~10pts in 10 years

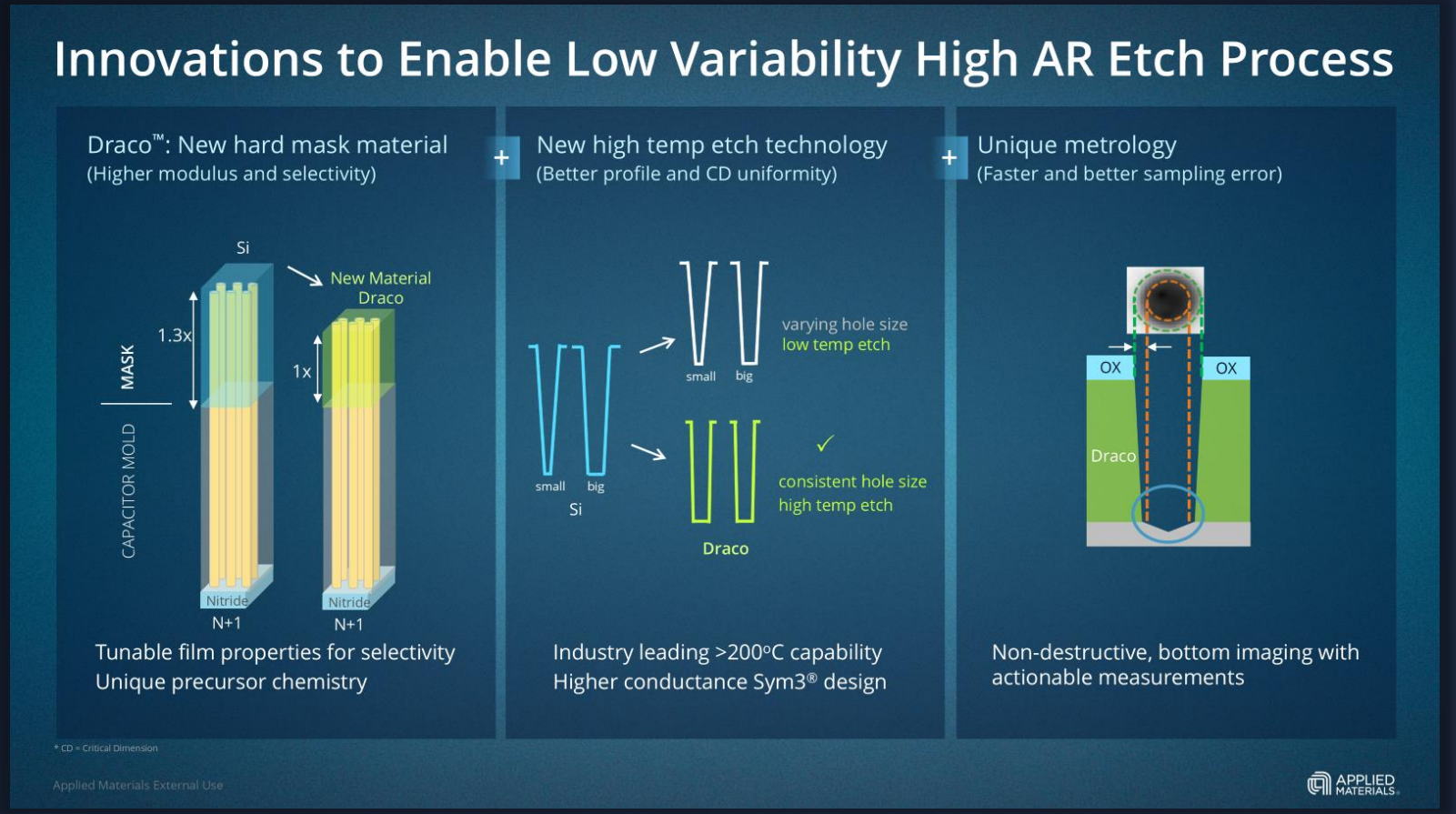


HBM

- Ported transistor integrated materials solutions from logic to DRAM to increase DRAM I/O speed
- Gained share in DRAM EUV patterning with co-optimized Draco™ CVD and Sym3™ etch for capacitor scaling
- Largest supplier of advanced packaging solutions, enabling multiple generations of HBM

Source: TechInsights, Applied Materials analysis.

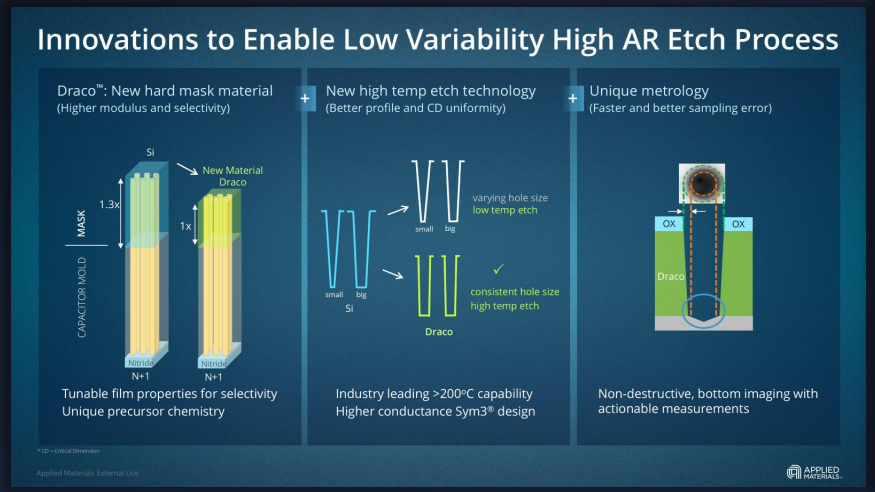
DRAM Case Study

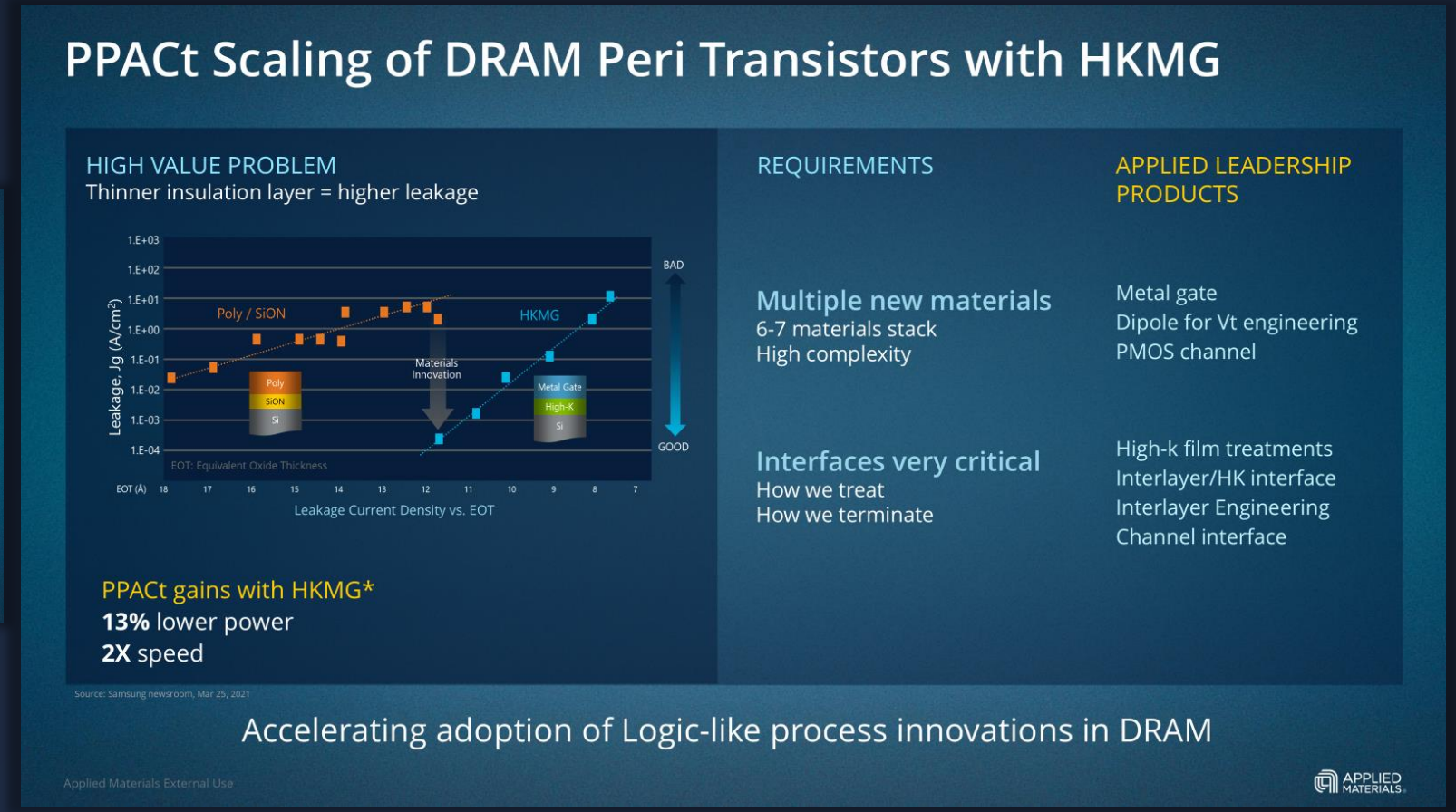


Over half a billion dollars in annual revenue

APPLIED MATERIALS

DRAM Case Study

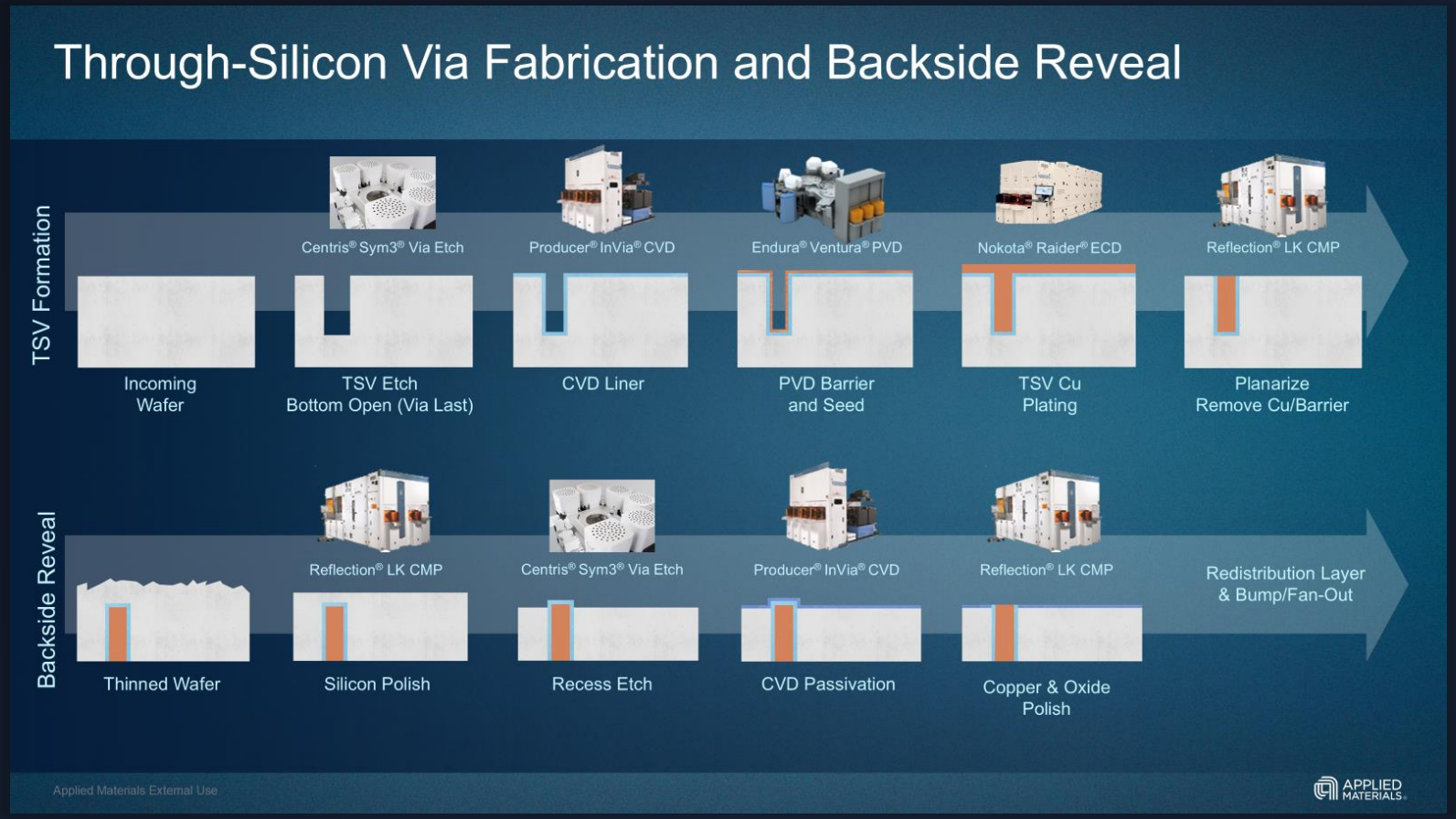




Over a billion dollars in annual revenue

APPLIED MATERIALS

Advanced Packaging Case Study



#1 in HBM packaging
Advanced packaging business growing >50%

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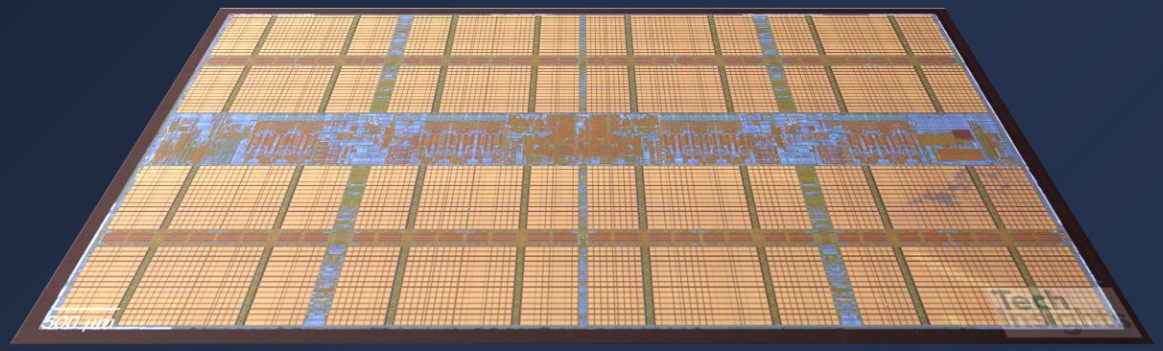
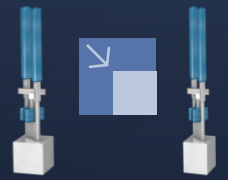
DRAM Inflections



DRAM Die

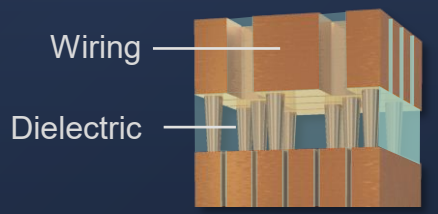
Source: TechInsights

6F² Scaling with EUV

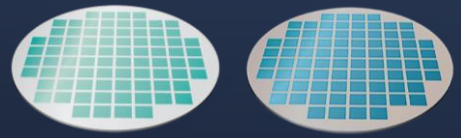


Advanced Periphery Transistors and Wiring

Planar FinFET



CMOS-Bonded Array



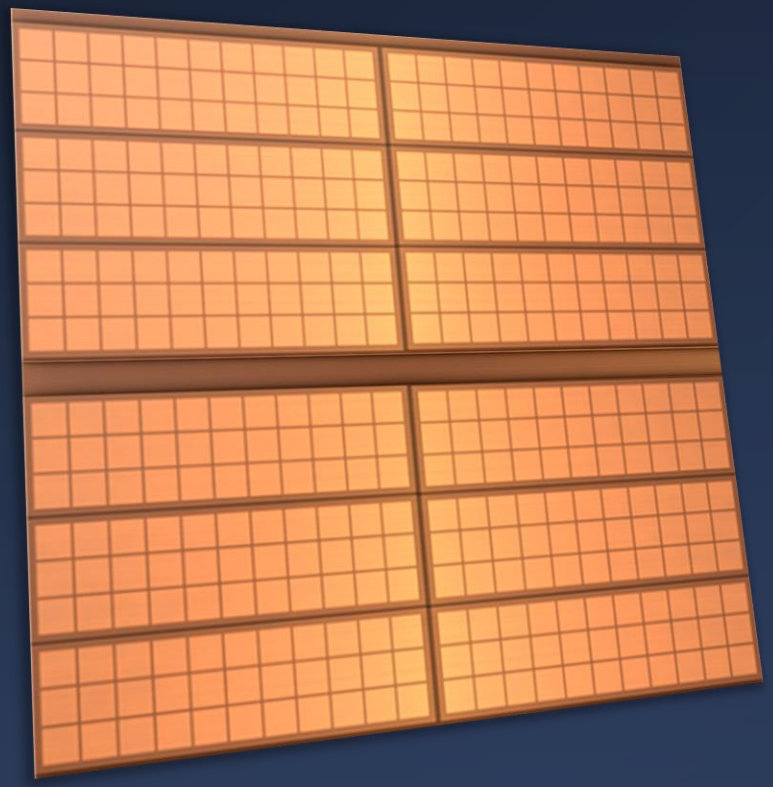
DRAM Arrays

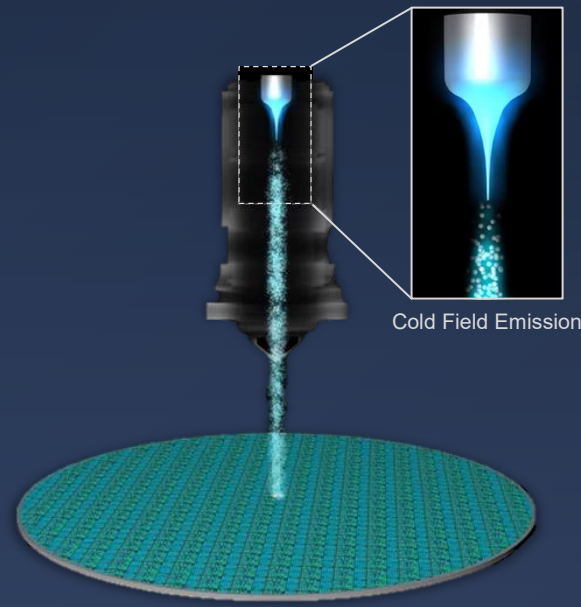
Peripheral Circuitry

4F² Architecture

3D DRAM

Advanced Packaging Inflections





Silicon Interposer

Panel

eBeam

Basic Computing Architecture

xPU

Processor

ALU
Arithmetic Logic Unit

CU
Control Unit

SRAM Cache
L1 / L2 / L3

Main Memory

DRAM

Data

Instructions

Address Space

I/O Devices

NAND SSD

Secondary Storage
NAND, HDD

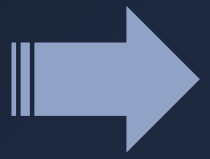
Input
Keyboard, Mouse
Scanner, Sensor

Output
Monitor, Printer
Speaker, LED

System Bus

Ideal Memory Characteristics

Low Latency



High Bandwidth

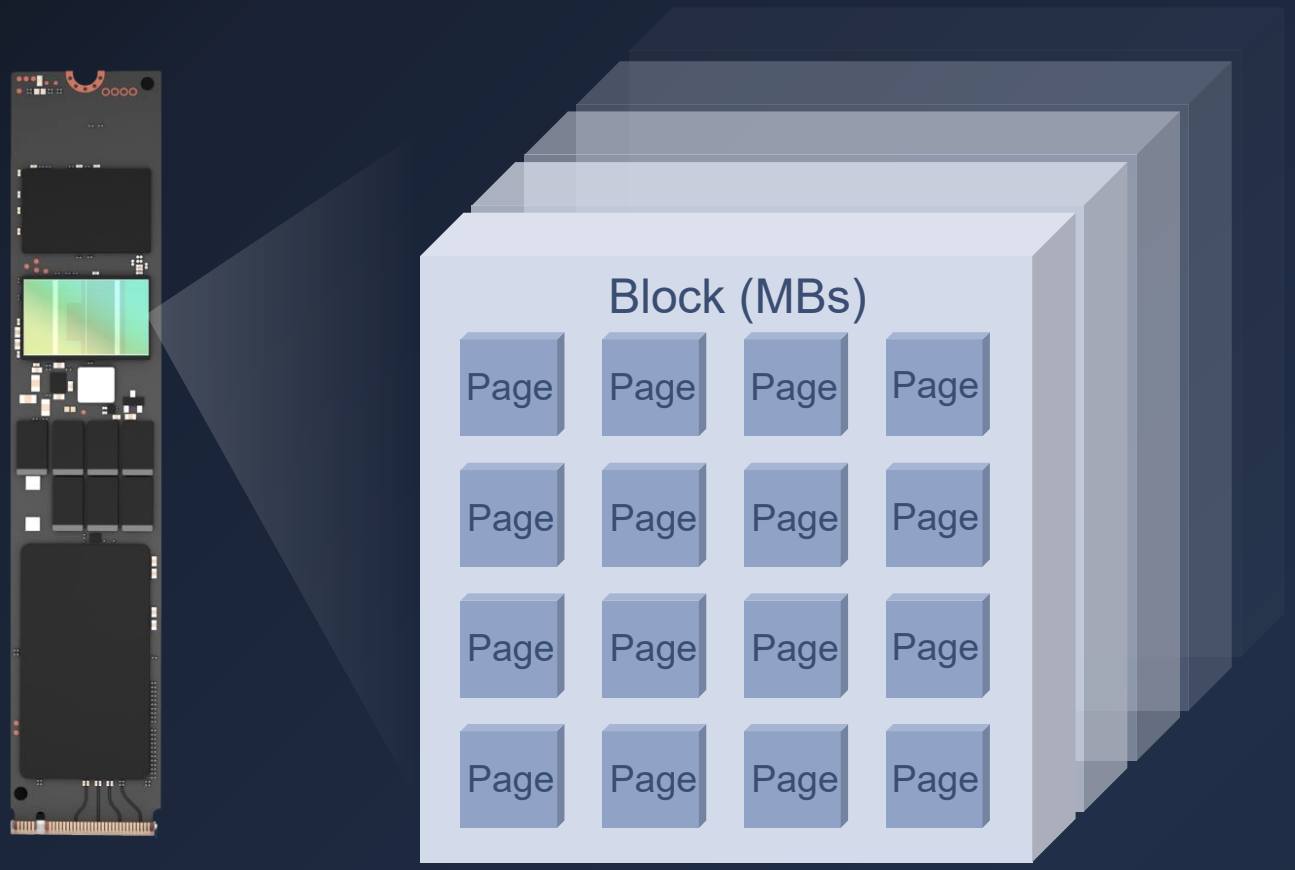
Random Access

Unlimited Endurance

Non-Volatile

Low Cost

NAND Tradeoffs



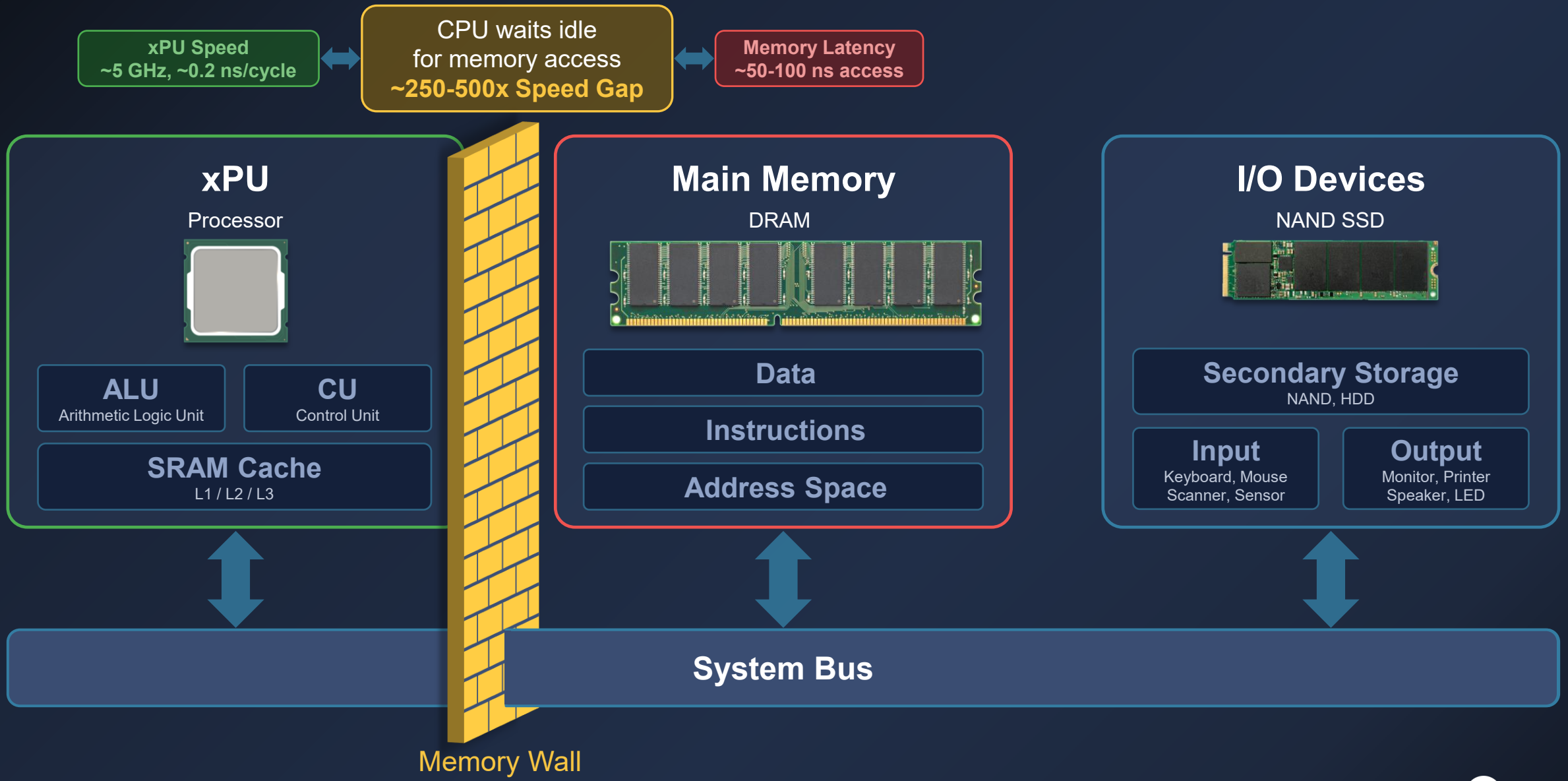
NAND Characteristics	
High Density	✓
Low Cost	✓
Page/Block Data Access	✗
Block Erase Only	✗
High Voltage Stress	✗

Memory Characteristics

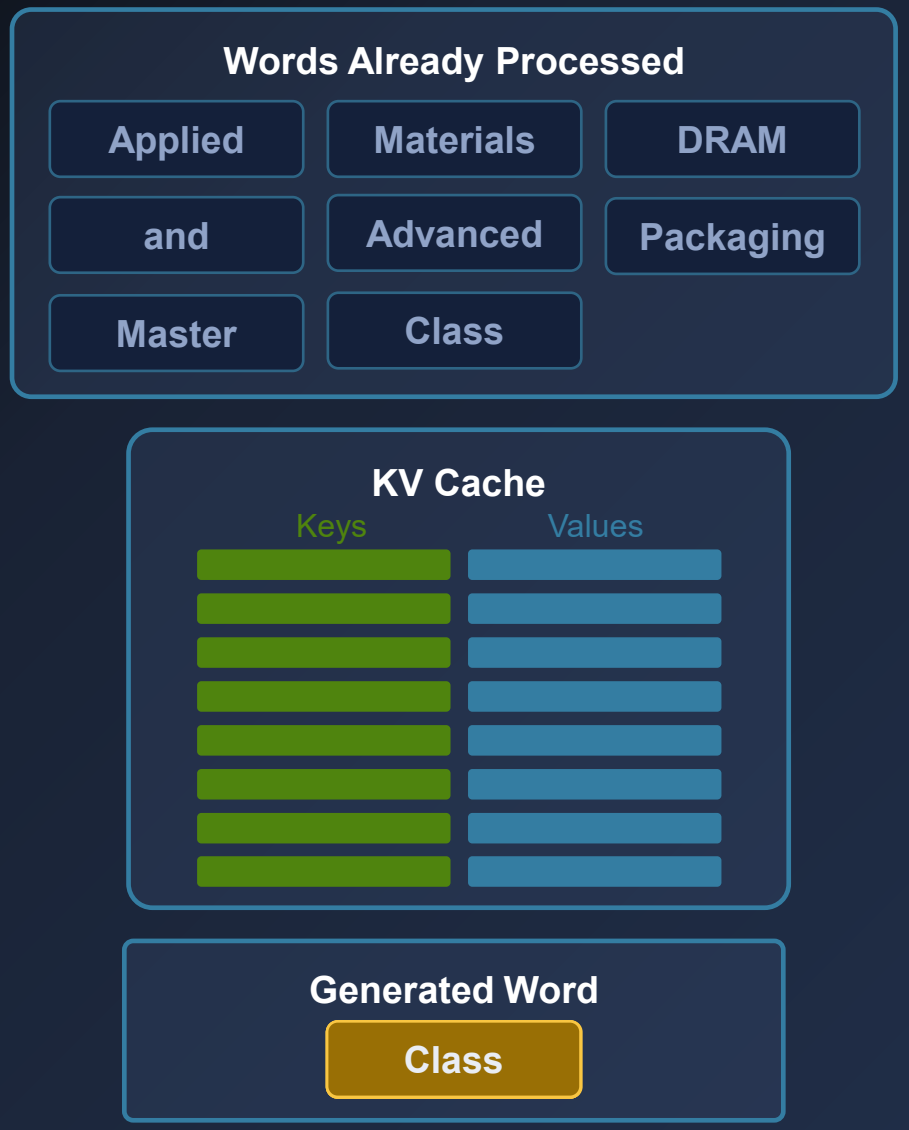
	Memory Type	Access Time*	Energy Use**
SRAM	SRAM Cache	1 second	1x
DRAM	High Bandwidth Memory	~10 seconds	~40x
	DDR DIMM	~1-2 minutes	~100x
NAND	SSD	Tens of hours	~1,000x

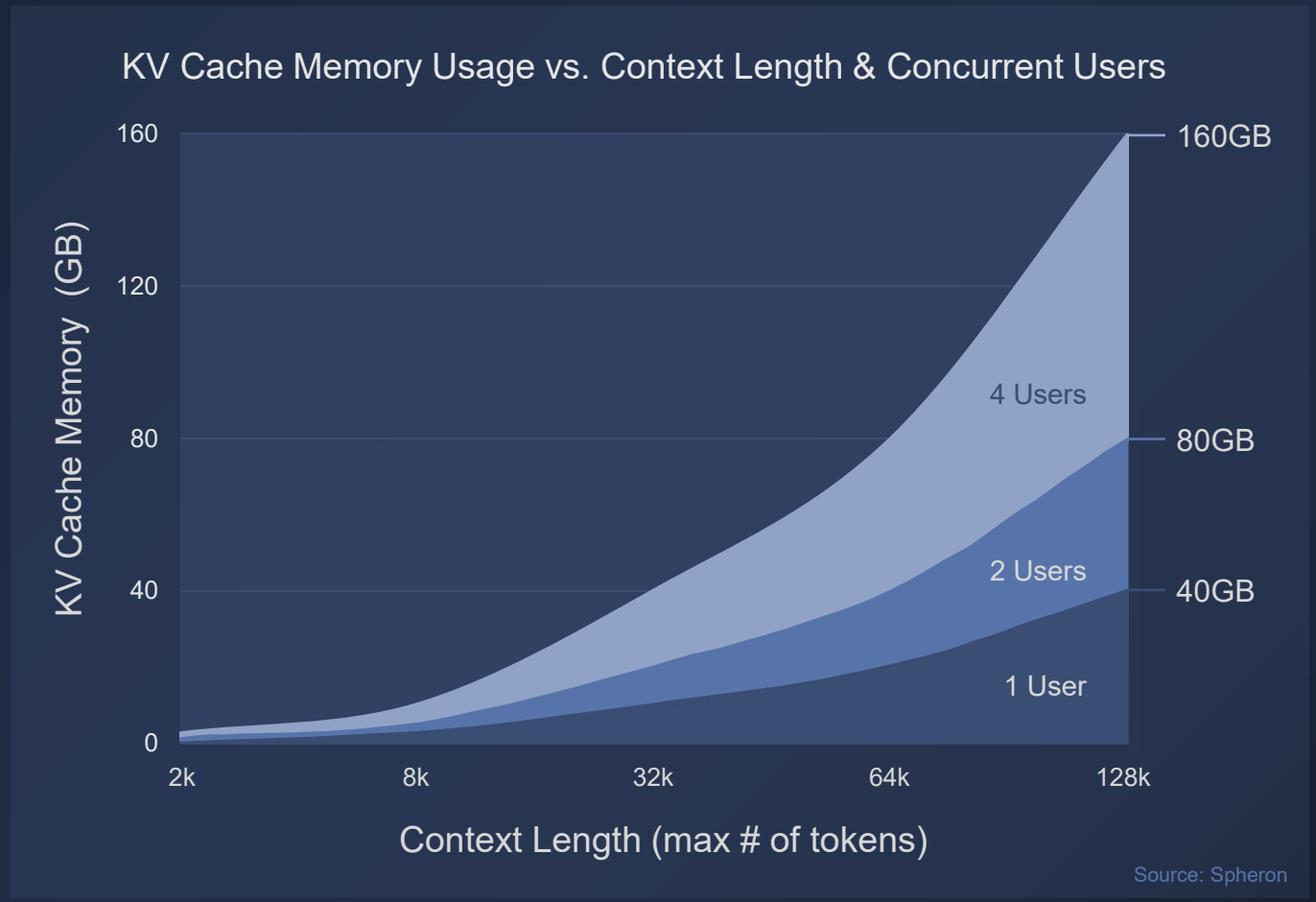
*Normalized access time per bit, with SRAM as baseline
**Normalized read energy per bit, with SRAM as baseline

Basic Computing Architecture



Memory and KV Cache Relationship





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Sony Varghese, Ph.D.

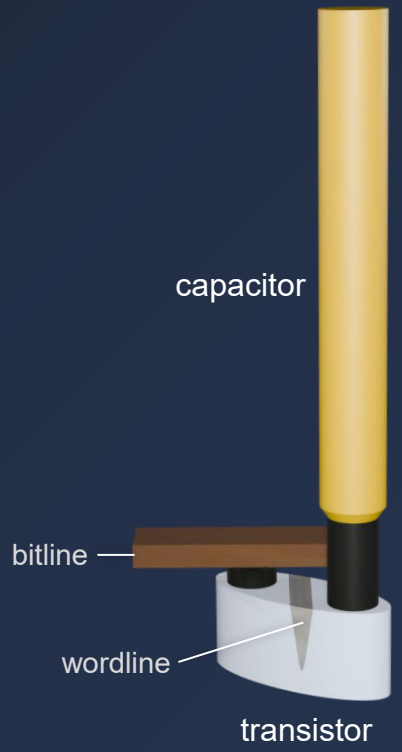
Managing Director
Technology Strategy
Semiconductor Products Group

APPLIED MATERIALS

DRAM Primer

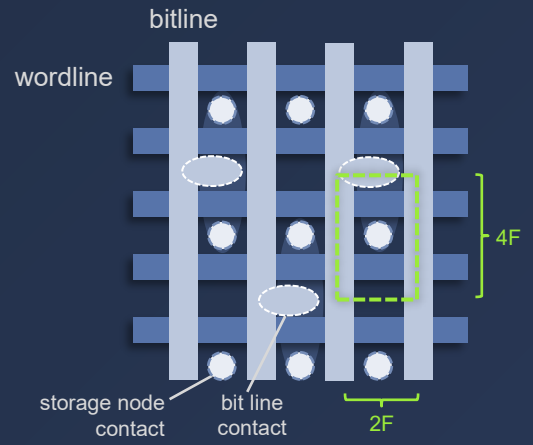
DRAM Cell

1T1C

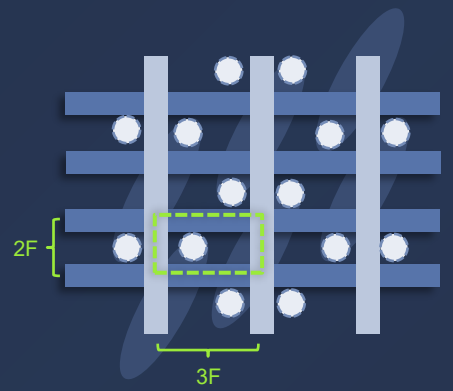


DRAM Cell Area

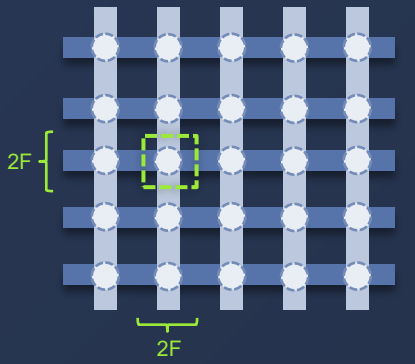
$8F^2$



$6F^2$



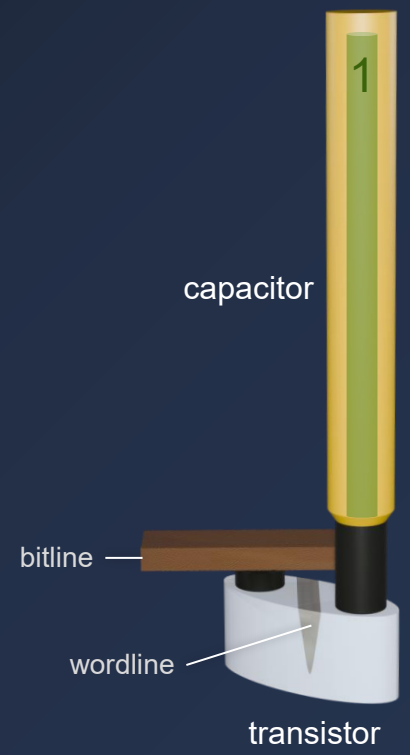
$4F^2$



DRAM Primer

DRAM Cell

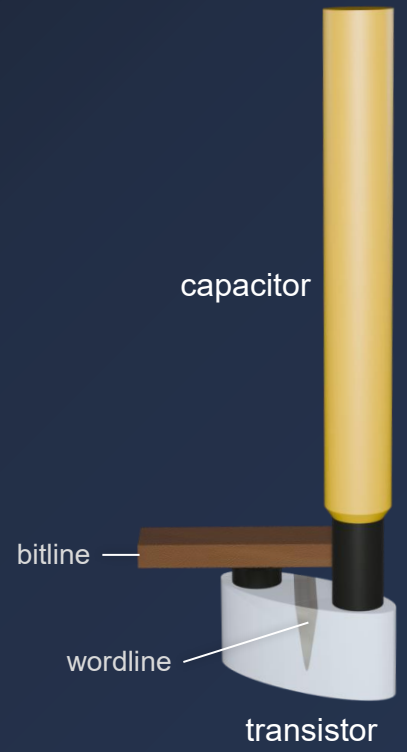
1T 1C



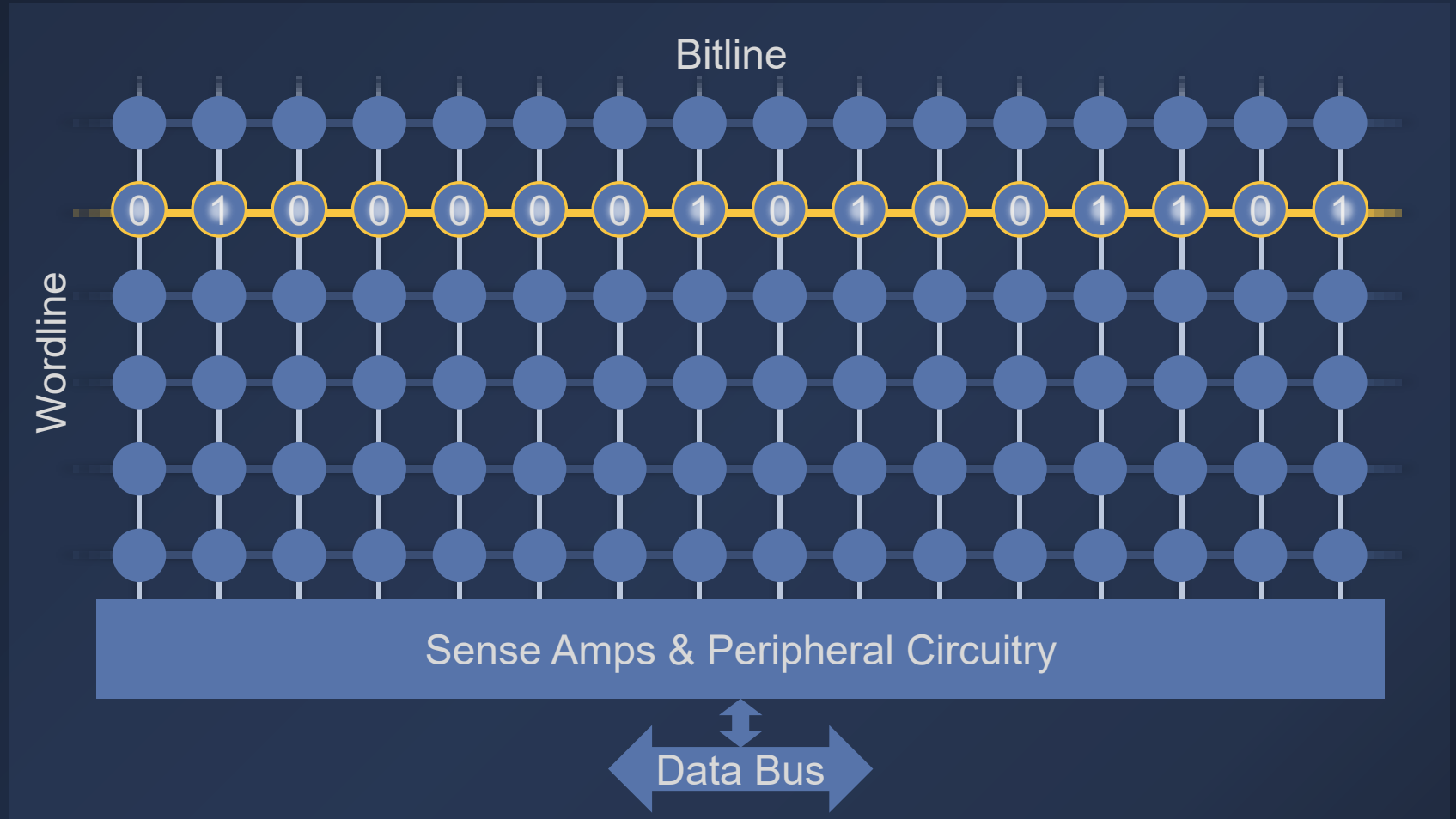
DRAM Primer

DRAM Cell

1T 1C

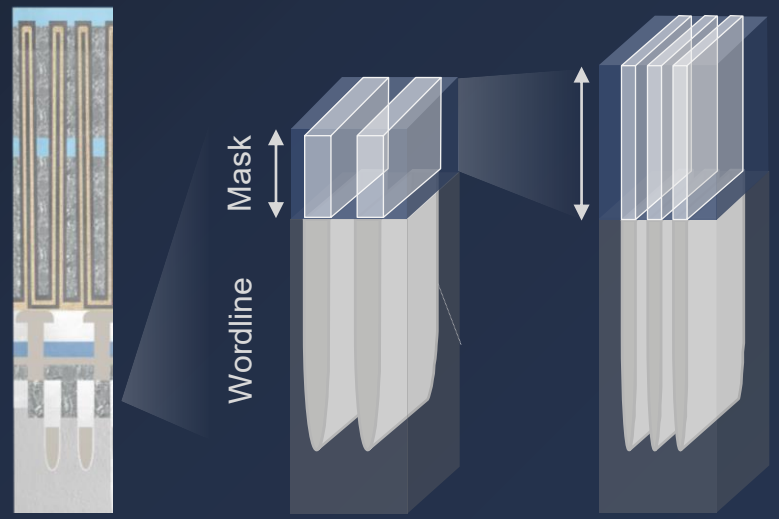


DRAM Array



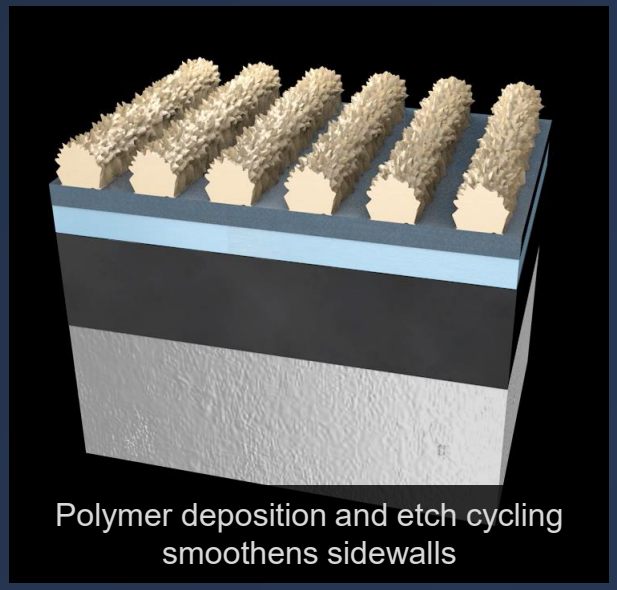
DRAM Inflection 1: EUV Scaling in $6F^2$

EUV scaling produces taller features



DRAM cell array

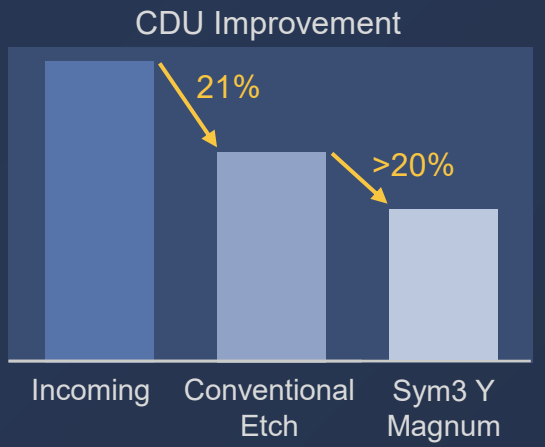
Improving EUV line patterns



Polymer deposition and etch cycling smoothens sidewalls

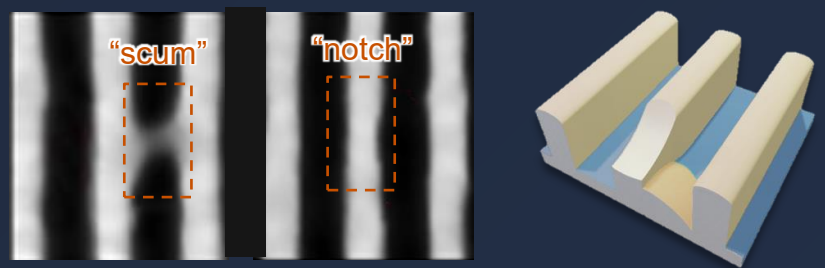
Applied: #1 in DRAM conductor etch

Sym3™ Y Magnum™ Etch



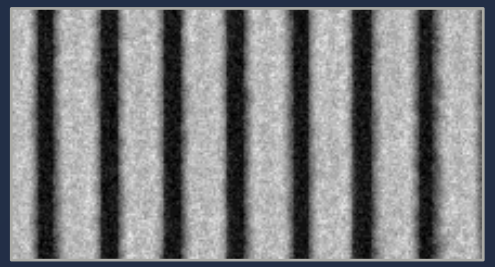
Higher photoresist etch variability and defects

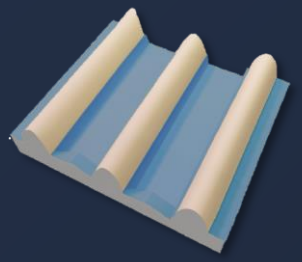
top view



Lower etch variability and defects

top view





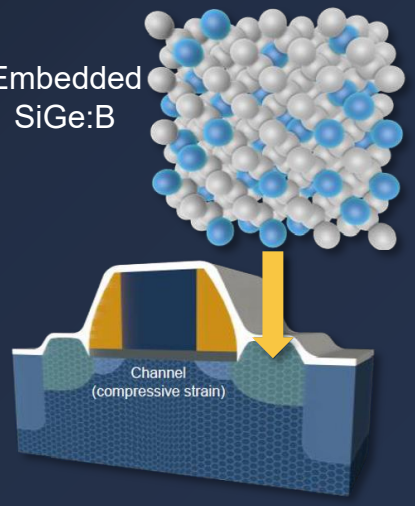
APPLIED MATERIALS

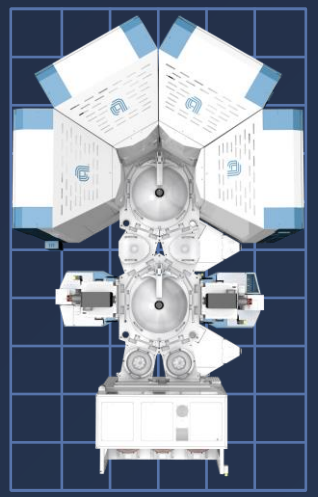
DRAM Inflection 2: Logic Technology Adoption

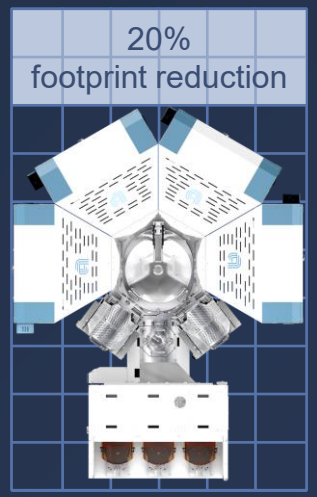
Epi

Centura™ Prime™ Epi

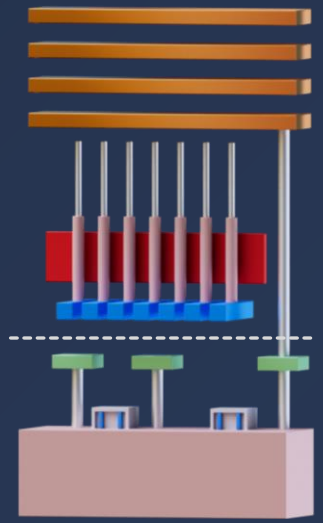
Embedded SiGe:B



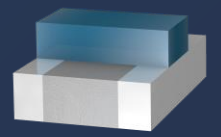




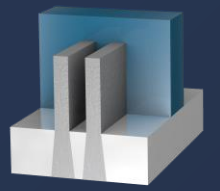
Interconnect



Periphery Logic → FinFET



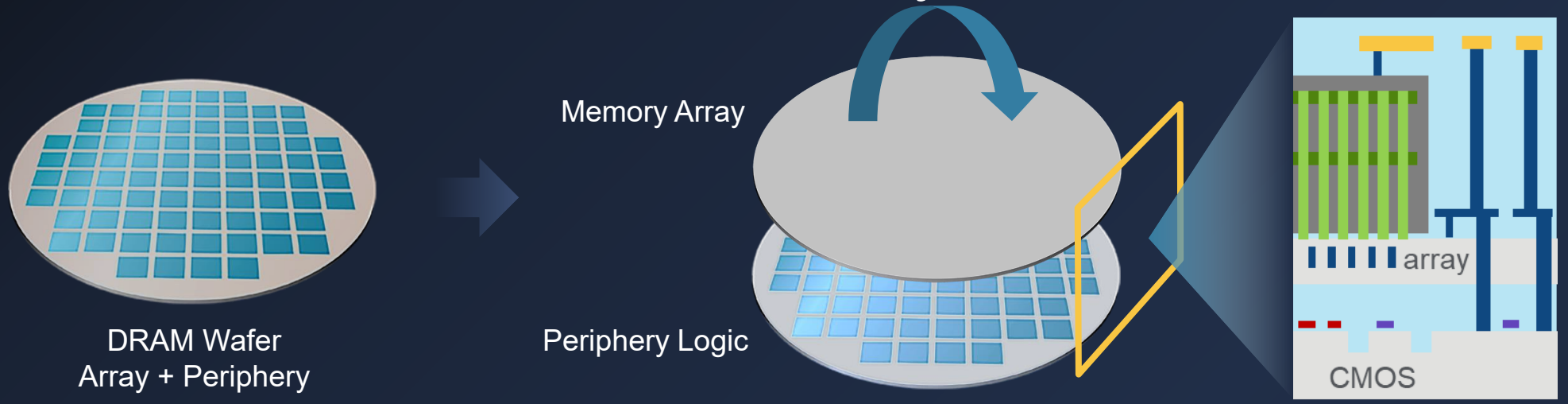
High-K Metal Gate
Planar FET



FinFET

APPLIED MATERIALS

DRAM Inflection 3: CMOS-Bonded Array



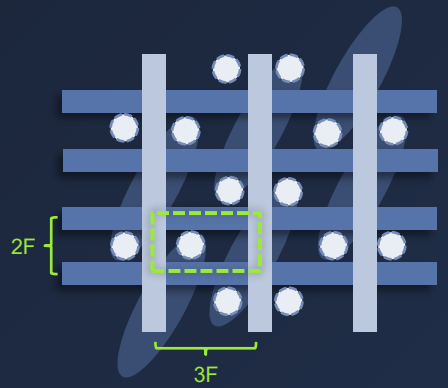
DRAM Wafer
Array + Periphery

	Conventional DRAM	CMOS-Bonded Array	
	Array + Periphery	**Memory Array Wafer**	**Periphery Logic**
Density and Efficiency	Die density 1x Cell efficiency ~60%	Die density ~1.4x Cell efficiency ~80%	Same die size as array More transistors
Transistor Performance	Cell 1x CMOS 1x	Cell 1x	CMOS >1x (lower thermal budget, less deactivation)
Interconnect	4-6 layers	1-3 layers	4-6 layers

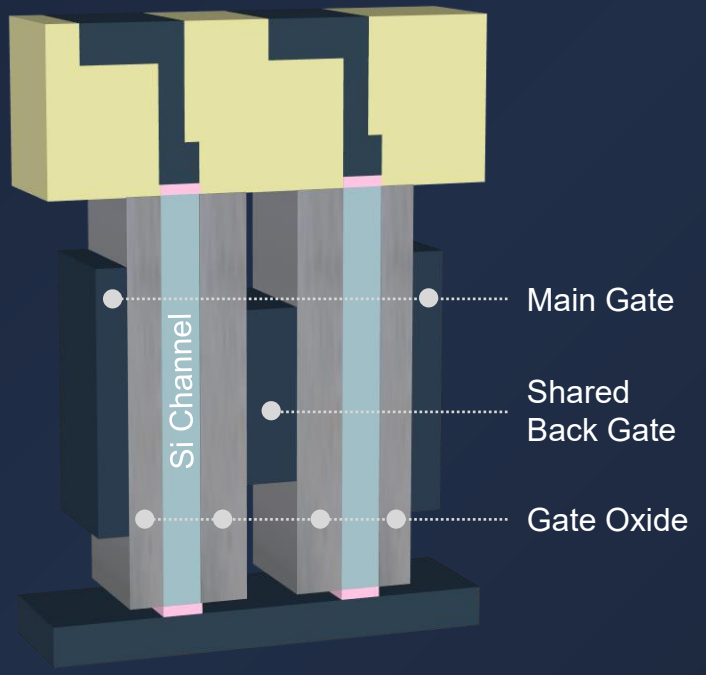
Source: K. Lee et al. / Samsung, T17.4, VLSI 2024

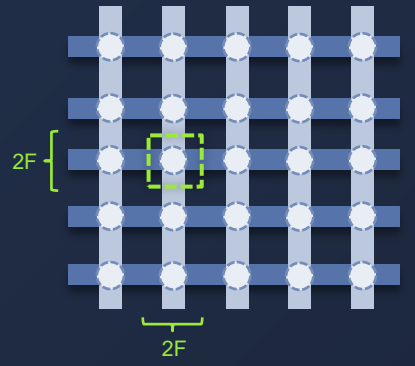
DRAM Inflection 4: $4F^2$ Architecture

$6F^2$ BCAT Transistor



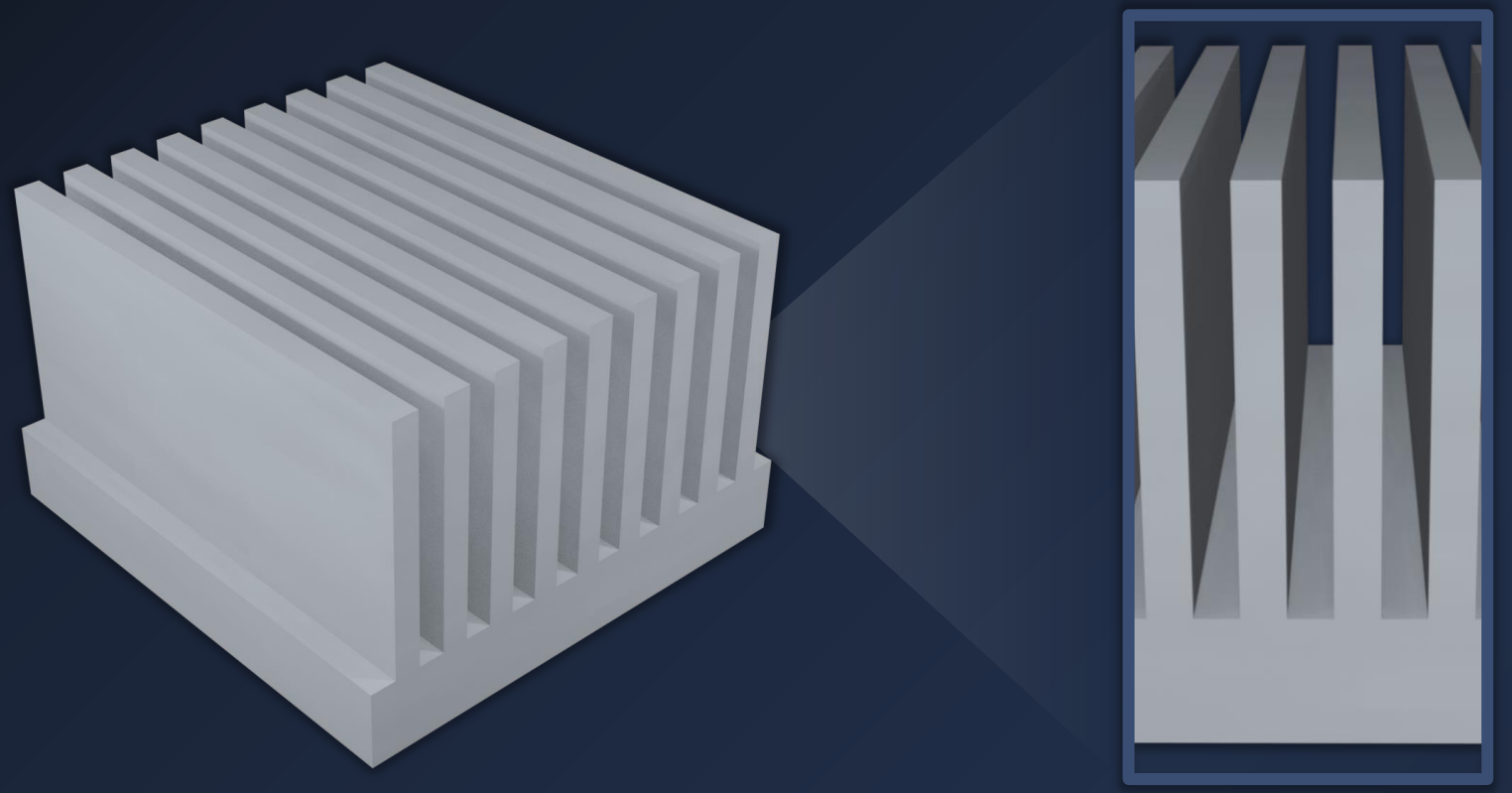
$4F^2$ Vertical Transistor





BCAT: Buried Channel Array Transistor

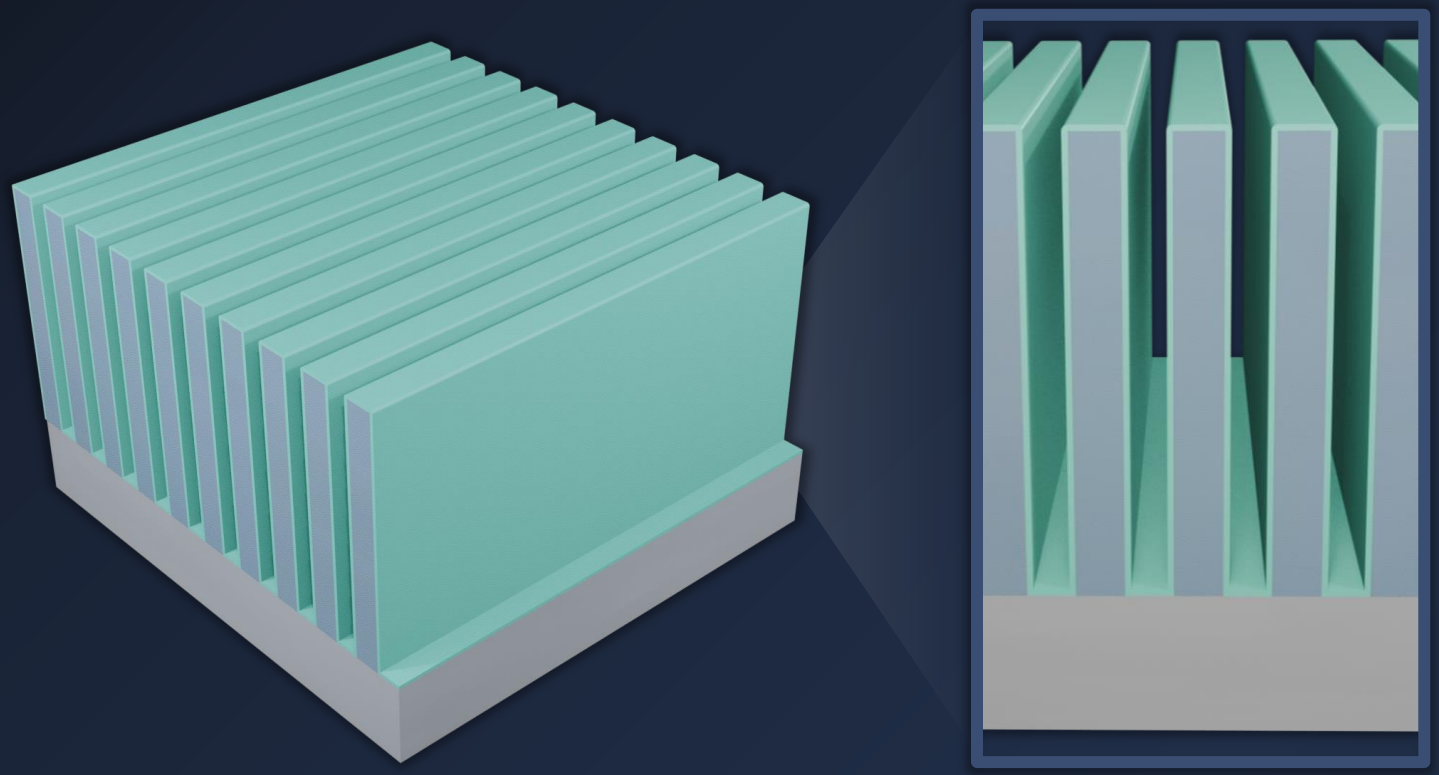
DRAM Inflection 4: Vertical Cell Transistors | Channel Etching



Shallow Trench Isolation Etch

Sym3™ Z Magnum™ Etch

DRAM Inflection 4: Vertical Cell Transistors | Gate Oxide

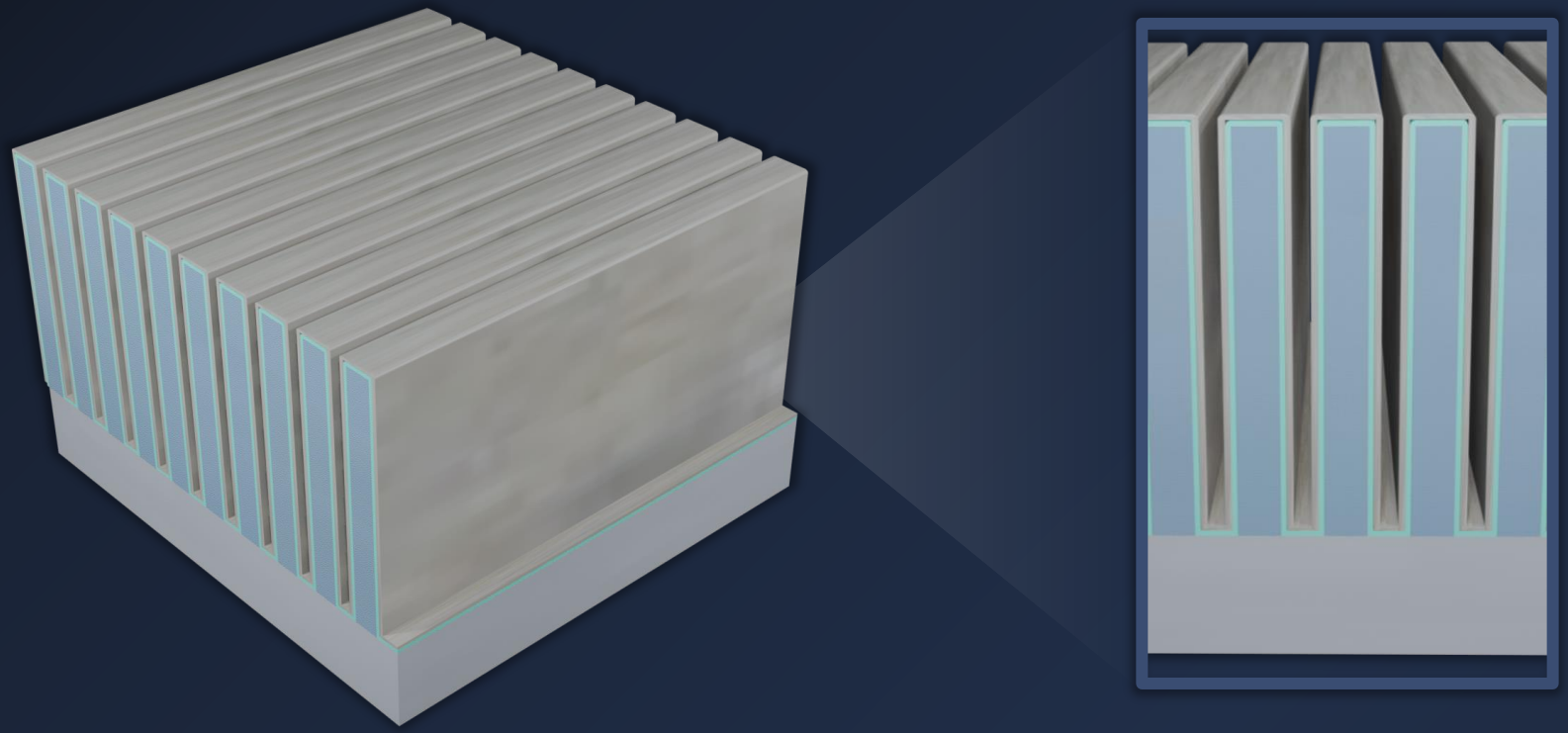


Gate Oxide Treatment

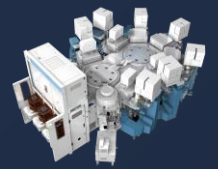
- ALD Oxide Deposition
- Oxide Densification
- Oxide Interface Treatment
- Conformal Nitridation

- Centura™ DPX™ Treatment
- Centura™ RPO2™ Radiance™ Treatment
- Centura™ DPX™ Treatment

DRAM Inflection 4: Vertical Cell Transistors | Metal Gate Stack

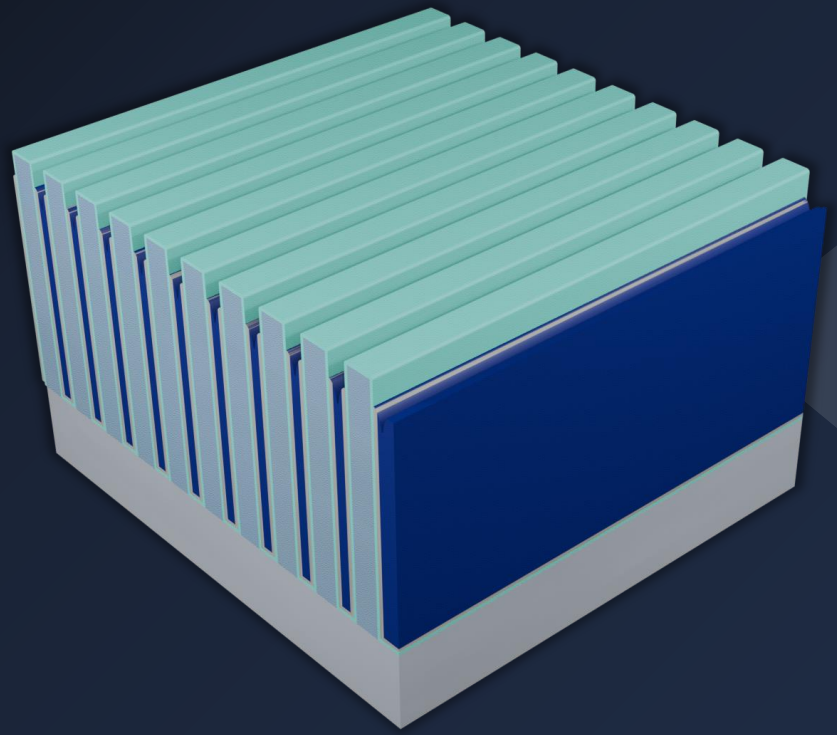


Gate Metal Deposition

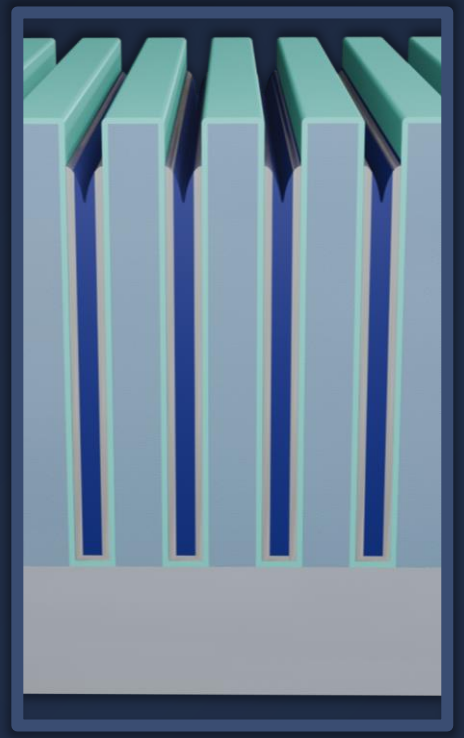


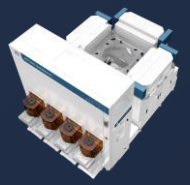
Endura™ Trillium™ ALD

DRAM Inflection 4: Vertical Cell Transistors | Buried Metal Gate



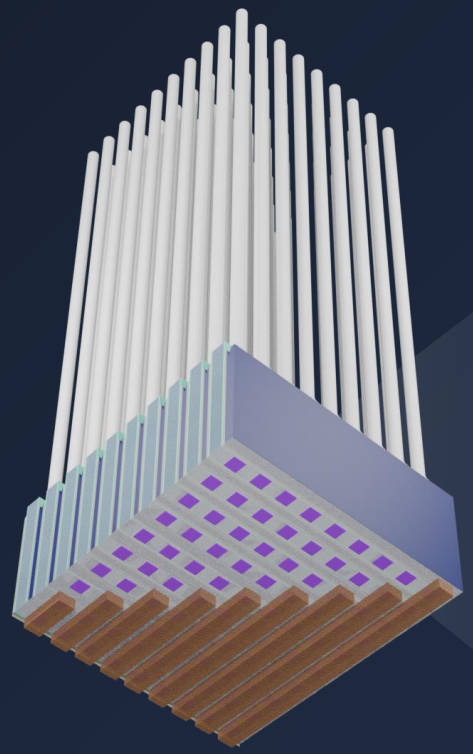
Gate Recess



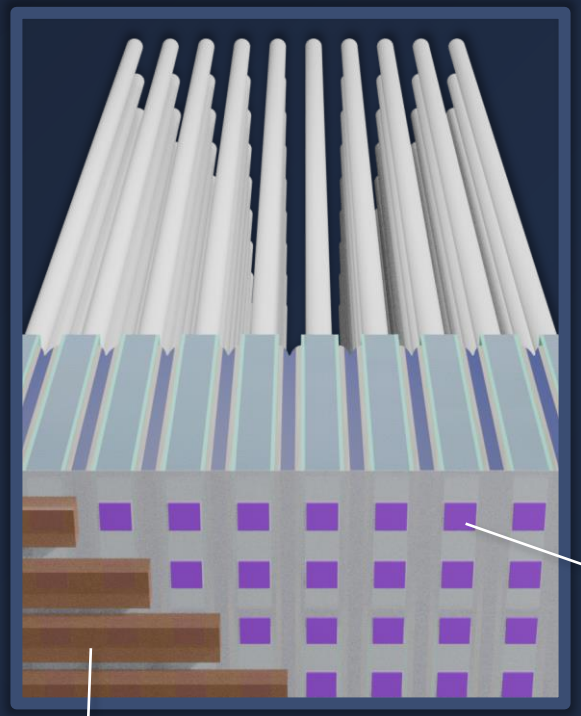


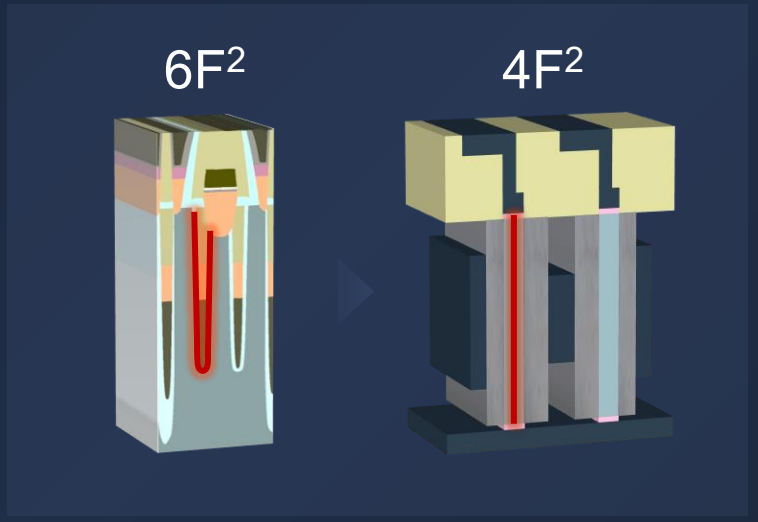
Producer™ Selectra™ Etch

DRAM Inflection 4: Vertical Cell Transistors | Bitline Junction



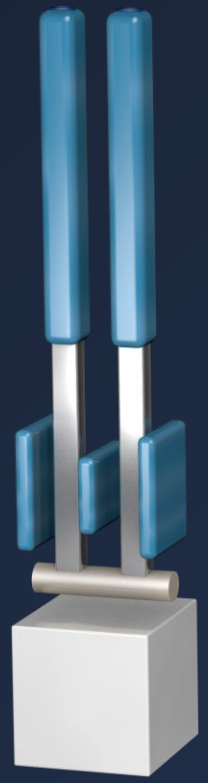
Bitline Junction

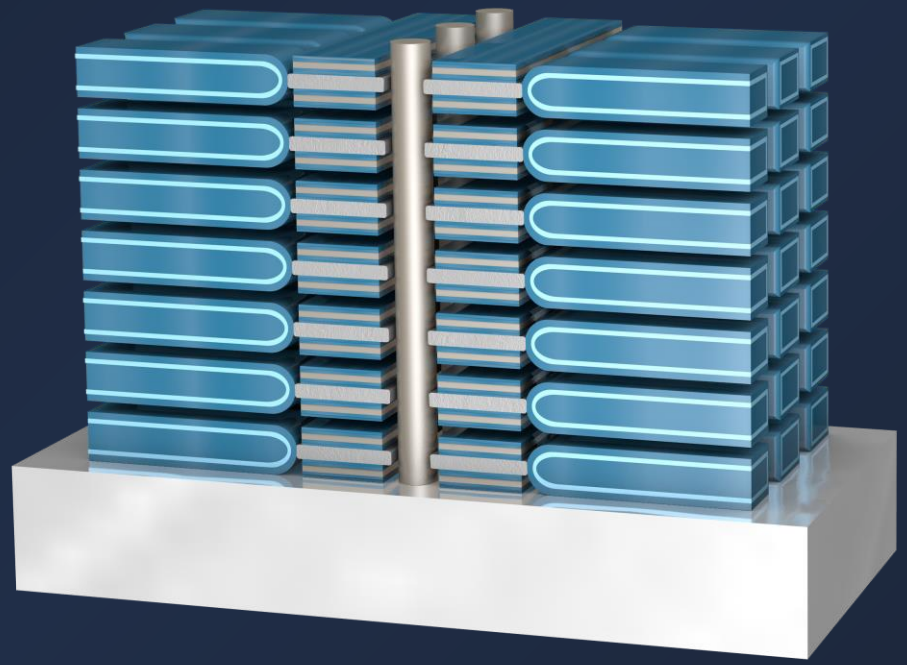




Low-Temp Selective Epi System

DRAM Inflection 5: 3D DRAM





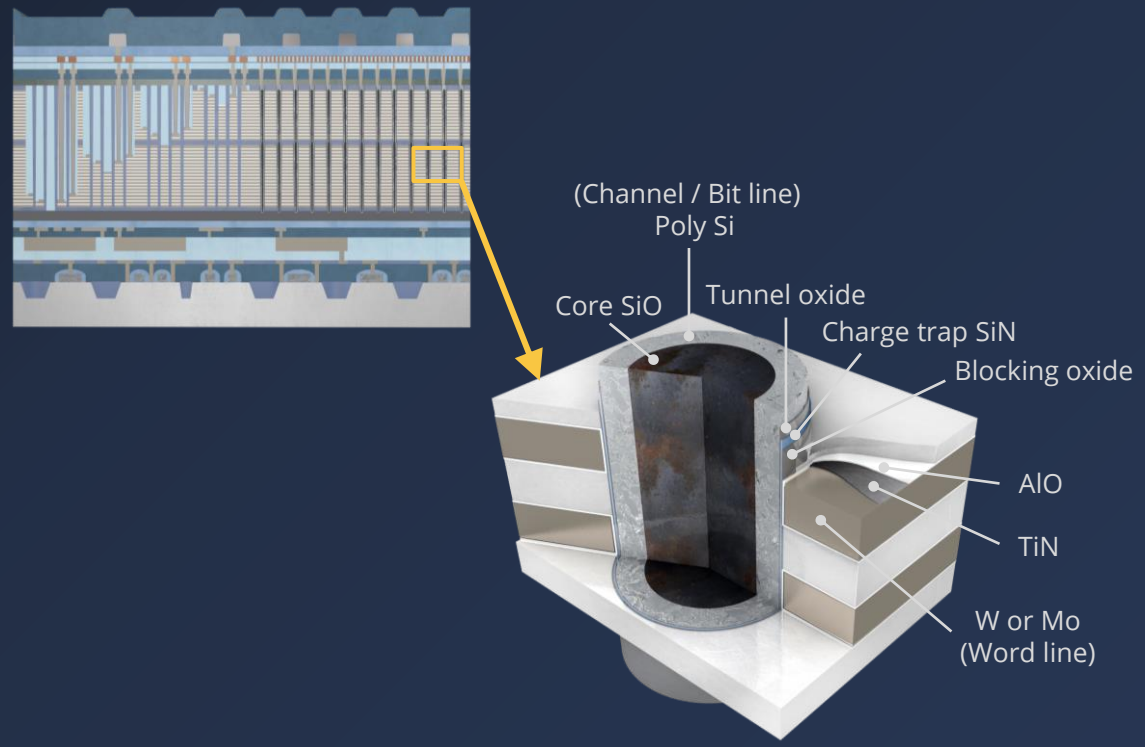
$6F^2$

$4F^2$

3D DRAM

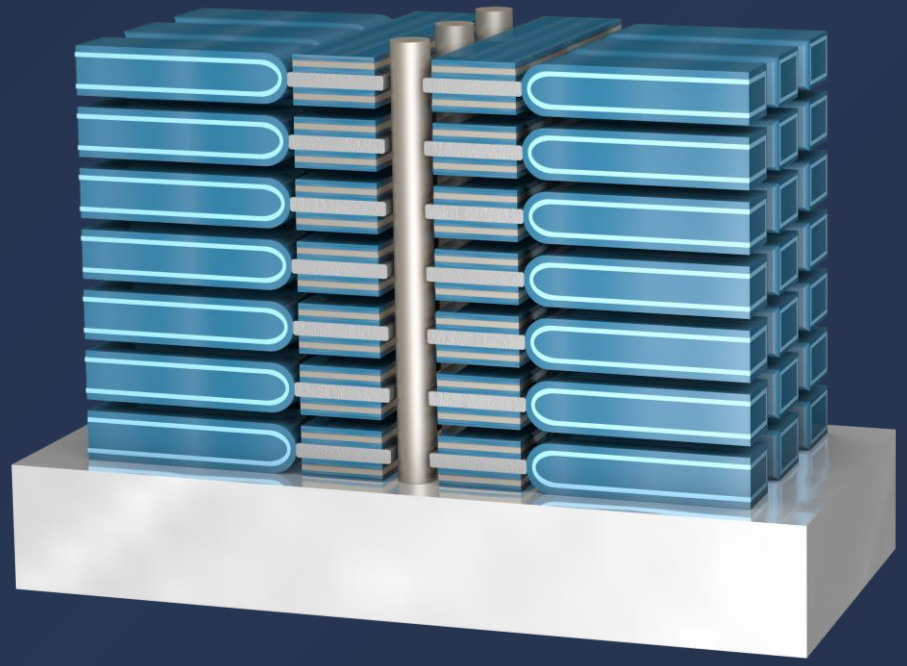
DRAM Inflection 5: 3D DRAM

3D NAND



Requires alternating layers of insulating dielectric material, and memory holes are formed using dielectric etch

3D DRAM



Relies heavily on conductor and metal stack deposition and lateral conductor etching

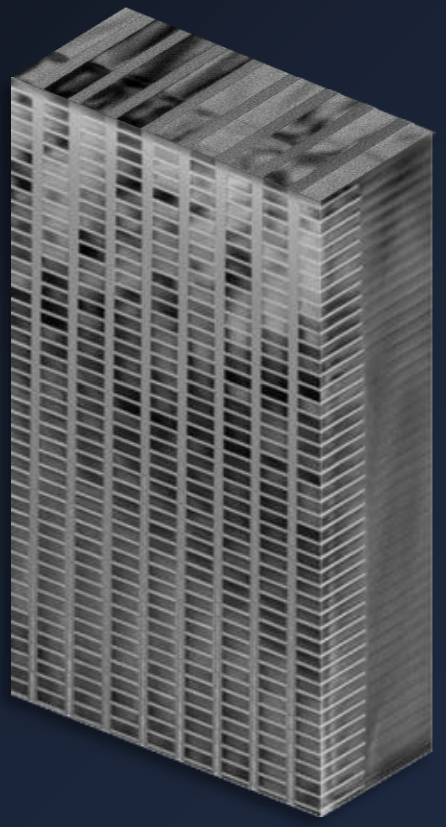
3D DRAM is very different from 3D NAND

EPIC CENTER

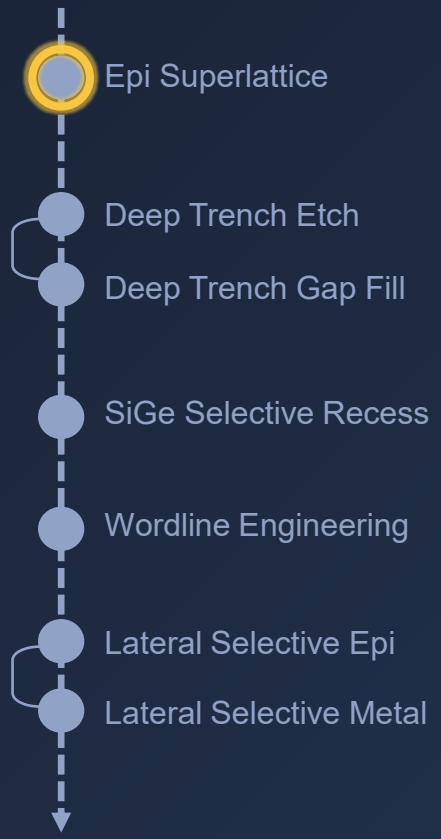
Collaborative platform for high-velocity innovation and commercialization of next-generation technology

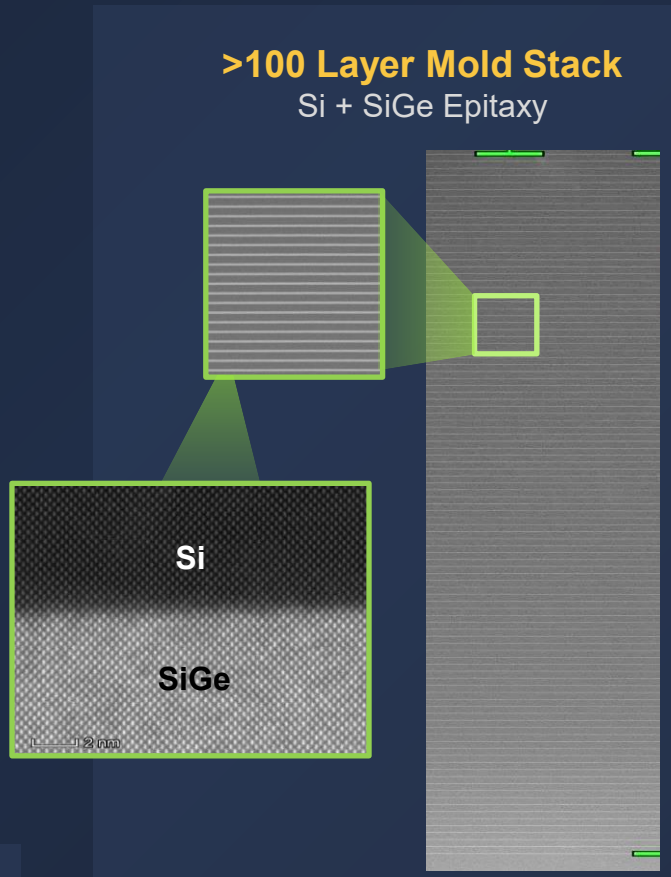
APPLIED MATERIALS

DRAM Inflection 5: 3D DRAM | Epi Superlattice



Applied Test Structure
for 3D DRAM





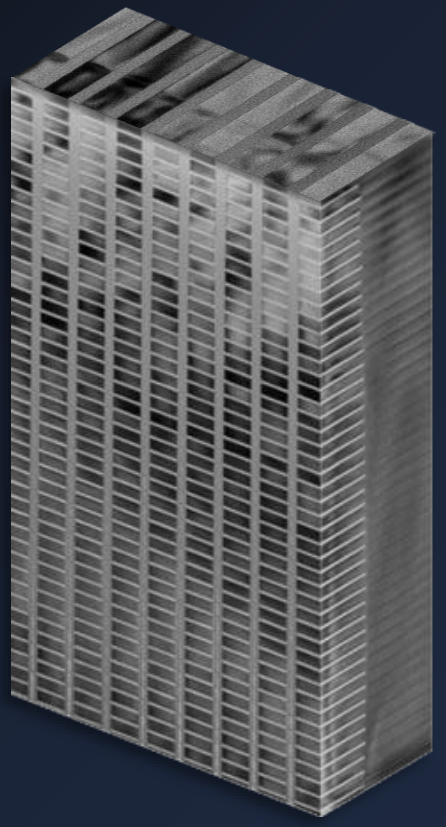
Tuned surface chemistry deliver defect-free, uniform interfaces

Strain engineering drives scaling to higher superlattice tier counts

Doped Epitaxy

APPLIED MATERIALS

DRAM Inflection 5: 3D DRAM | High-Aspect-Ratio Etch

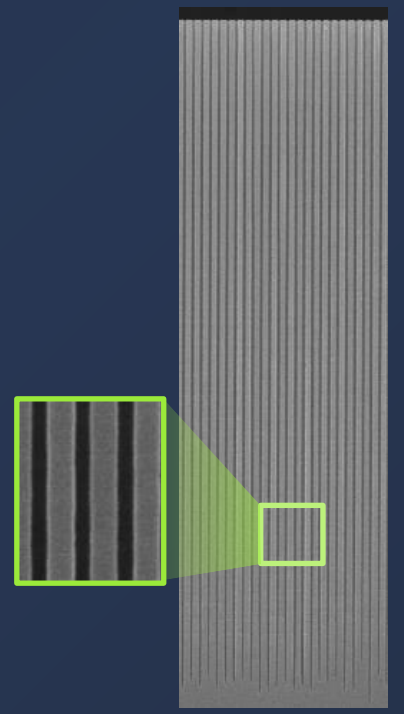


Applied Test Structure
for 3D DRAM

Co-optimized Processes

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- SiGe Selective Recess
- Wordline Engineering
- Lateral Selective Epi
- Lateral Selective Metal

High Aspect Ratio Si Etch
>150:1 aspect ratio

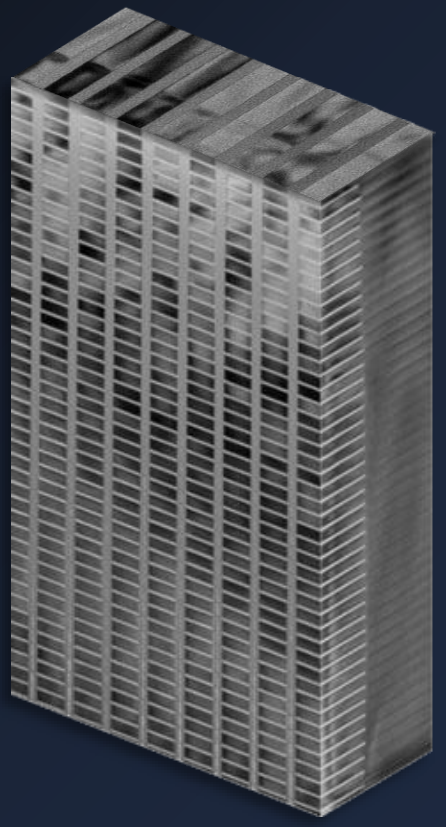


Hardware innovations enable precise uniformity and depth control

Sym3™ Conductor Etch

APPLIED MATERIALS

DRAM Inflection 5: 3D DRAM | High-Aspect-Ratio Gap Fill

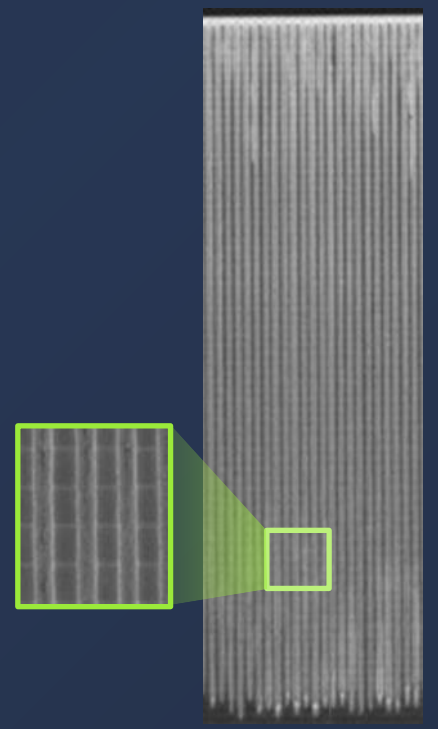


Applied Test Structure
for 3D DRAM

Co-optimized Processes

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- SiGe Selective Recess
- Wordline Engineering
- Lateral Selective Epi
- Lateral Selective Metal

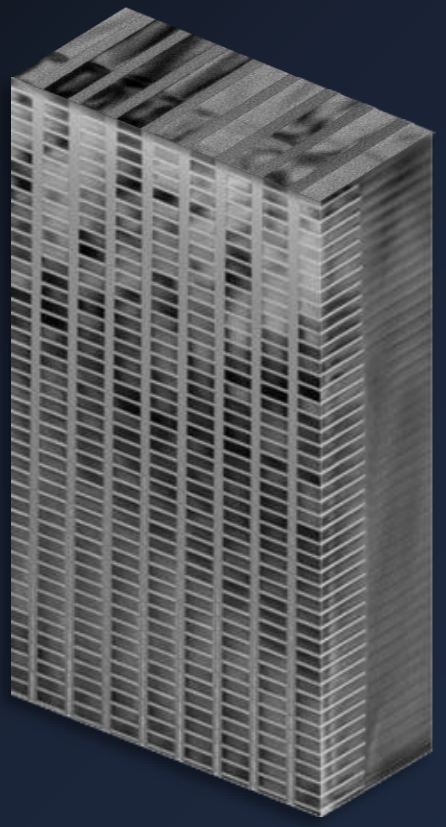
High Aspect Ratio Gap Fill
>150:1 aspect ratio



Void-free gap fill ensures strong isolation and structural support

ALD Oxide

DRAM Inflection 5: 3D DRAM | Selective Lateral Recess

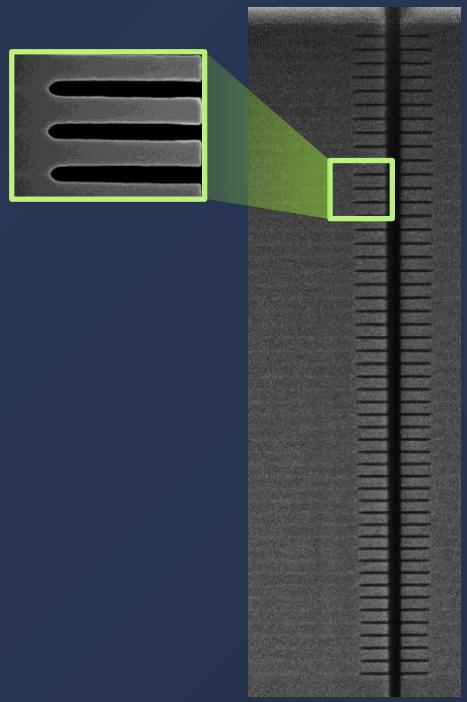


Applied Test Structure
for 3D DRAM

New Process Technology

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- **SiGe Selective Recess**
- Wordline Engineering
- Lateral Selective Epi
- Lateral Selective Metal

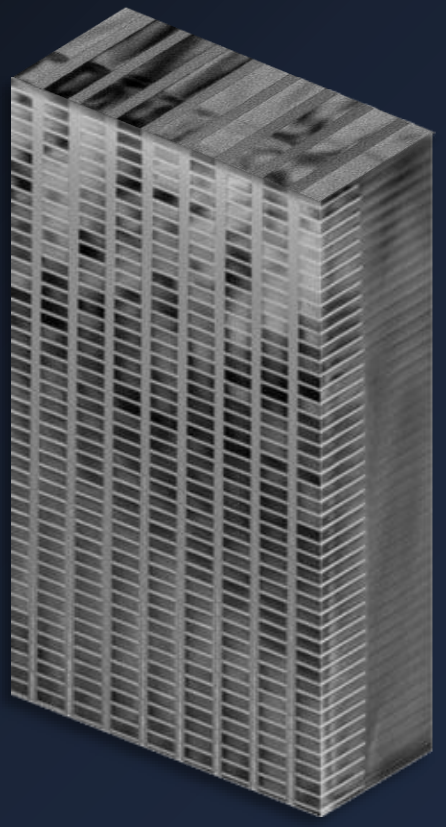
Lateral SiGe Recess
>100:1 selectivity



Highly selective etch removes SiGe
while preserving surrounding materials

Selective Etch

DRAM Inflection 5: 3D DRAM | Wordline Engineering



Applied Test Structure
for 3D DRAM

New Process Technology

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- SiGe Selective Recess
- **Wordline Engineering**
- Lateral Selective Epi
- Lateral Selective Metal

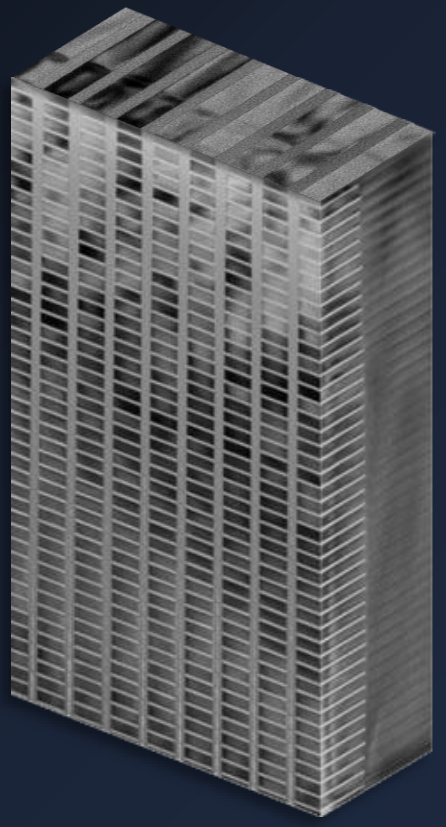
Wordline Engineering

Engineered metal grain growth reduces wordline resistance

Producer™ Viva™
Radical Treatment

APPLIED MATERIALS

DRAM Inflection 5: 3D DRAM | Lateral Selective Epi

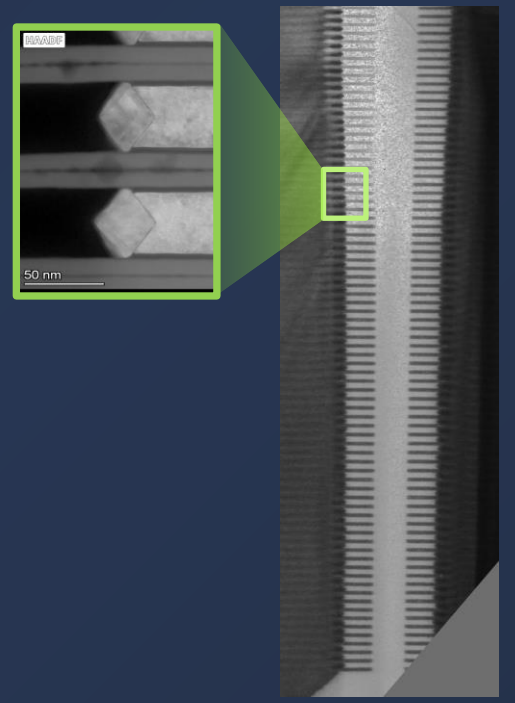


Applied Test Structure
for 3D DRAM

New Technologies Co-optimized

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- SiGe Selective Recess
- Wordline Engineering
- **Lateral Selective Epi**
- Lateral Selective Metal

Lateral Selective Epi

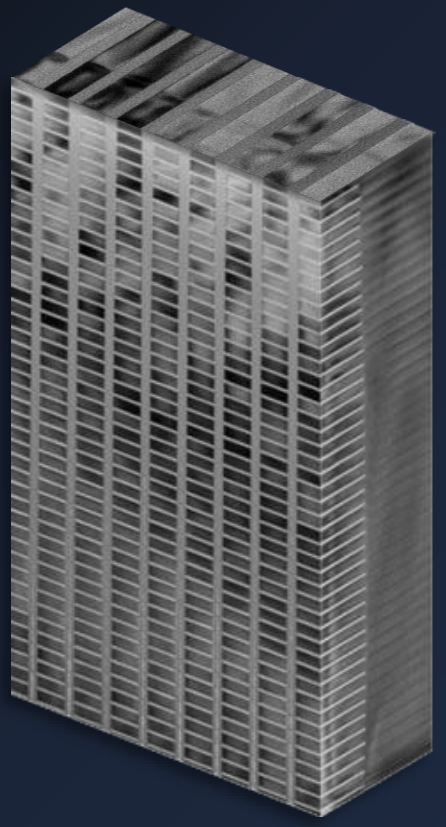


Non-line-of-sight process enables
junction doping and storage node contact formation

Centura™ Prime™ Epi

APPLIED MATERIALS

DRAM Inflection 5: 3D DRAM | Lateral Selective Epi

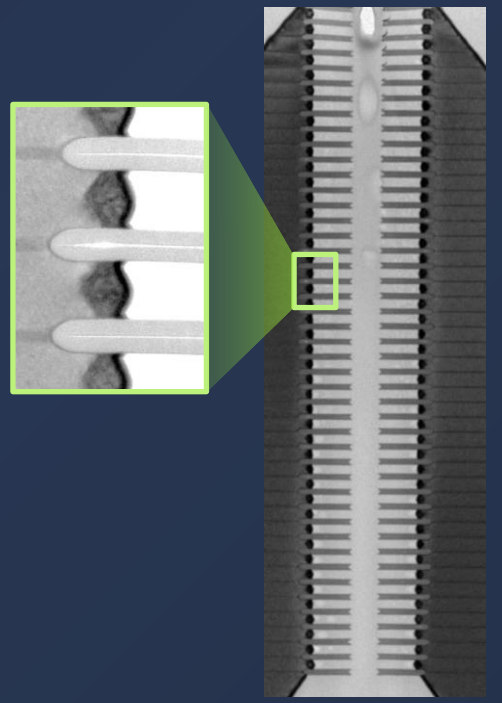


Applied Test Structure
for 3D DRAM

New Technologies Co-optimized

- Epi Superlattice
- Deep Trench Etch
- Deep Trench Gap Fill
- SiGe Selective Recess
- Wordline Engineering
- Lateral Selective Epi
- Lateral Selective Metal

Lateral Metal Deposition

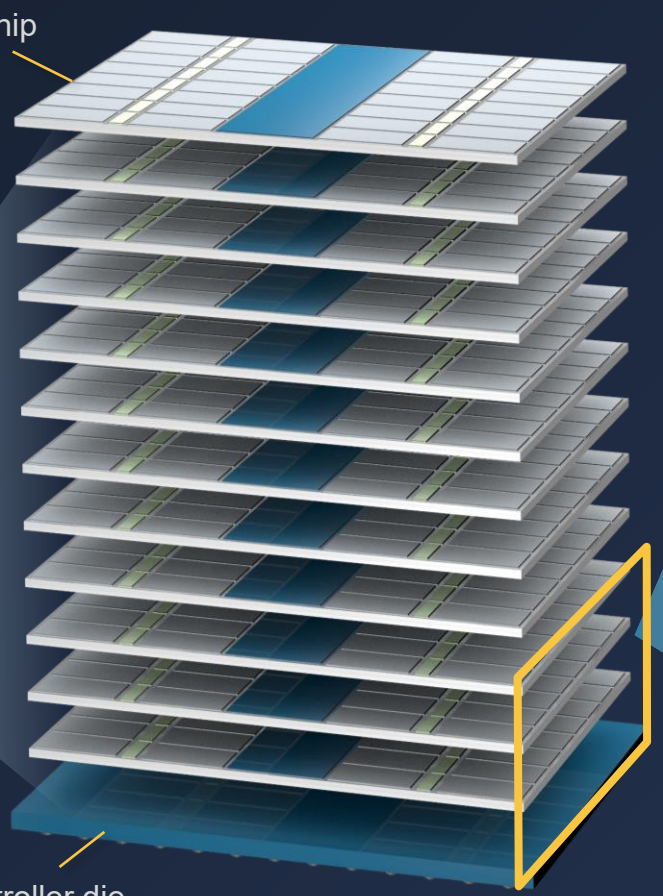


Advanced thermal deposition enables low-resistance contacts

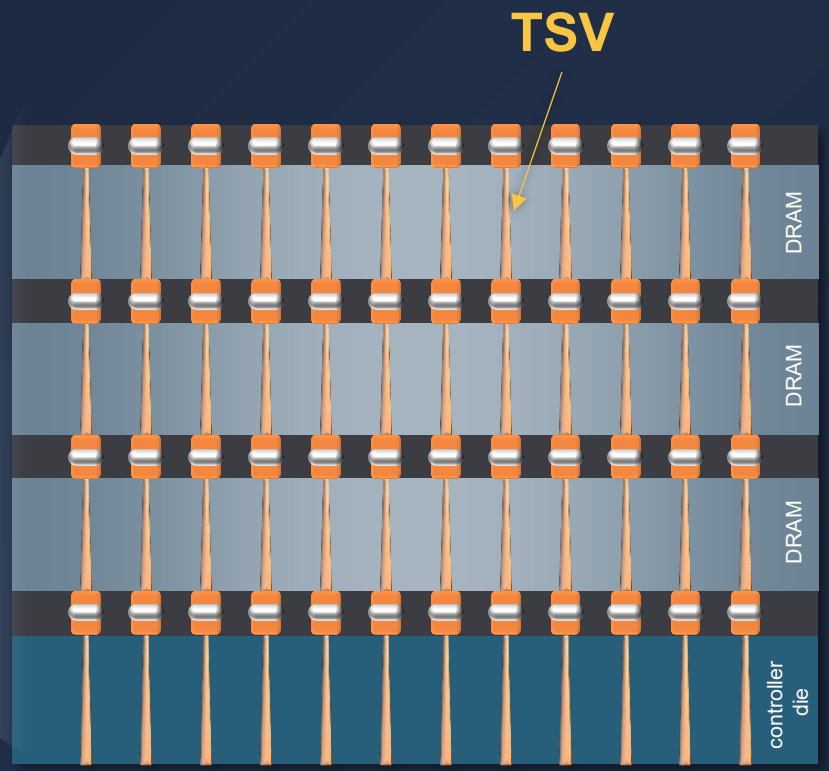
Selective Mo ALD

HBM: Stacked DRAM Dies

AI Accelerator



HBM Stack



HBM3: >>1024 I/O TSVs
HBM4: >>2048 I/O TSVs

DDR DRAM die: 64 I/O

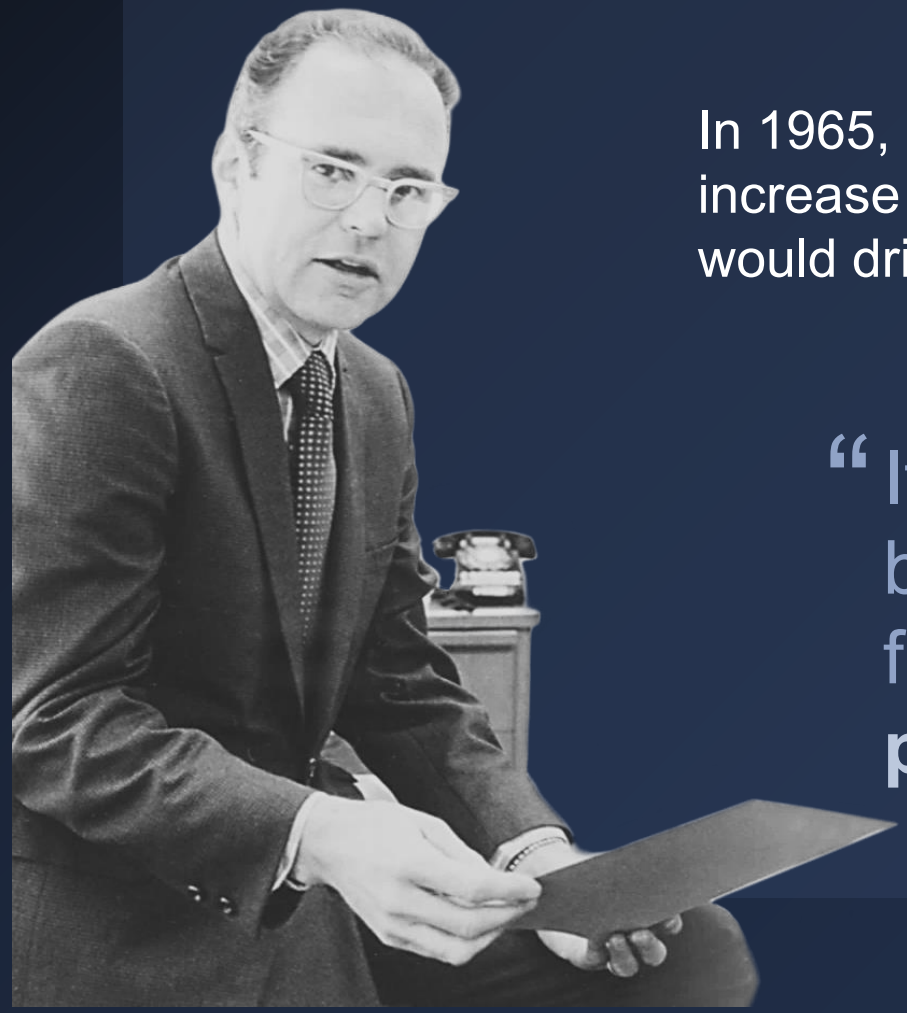
MASTER CLASS June 25, 2026

Jinho An, Ph.D.

Senior Director
Heterogeneous Integration
Semiconductor Products Group

APPLIED MATERIALS

More Than Moore



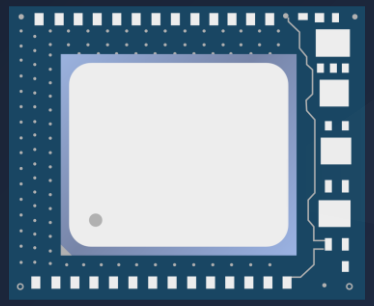
In 1965, Gordon Moore predicted both the exponential increase of transistors on a chip, and conditions that would drive *the disaggregation of the system-on-chip*.

> “It may prove to be more economical to build **large systems** out of smaller functions, which are **separately packaged and interconnected** ”

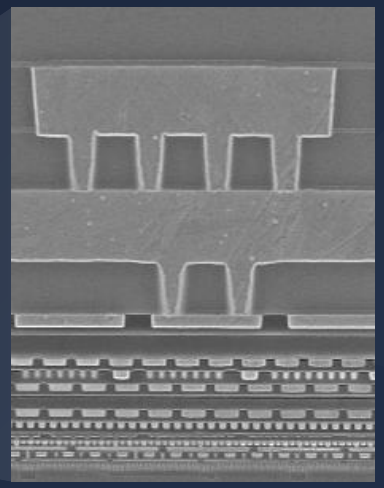
https://archive.computerhistory.org/resources/access/text/2017/03/102770822-05-01-acc.pdf

The System-on-a-Chip (SoC) Era

Server chip (SoC)



Microscope cross section view of chip

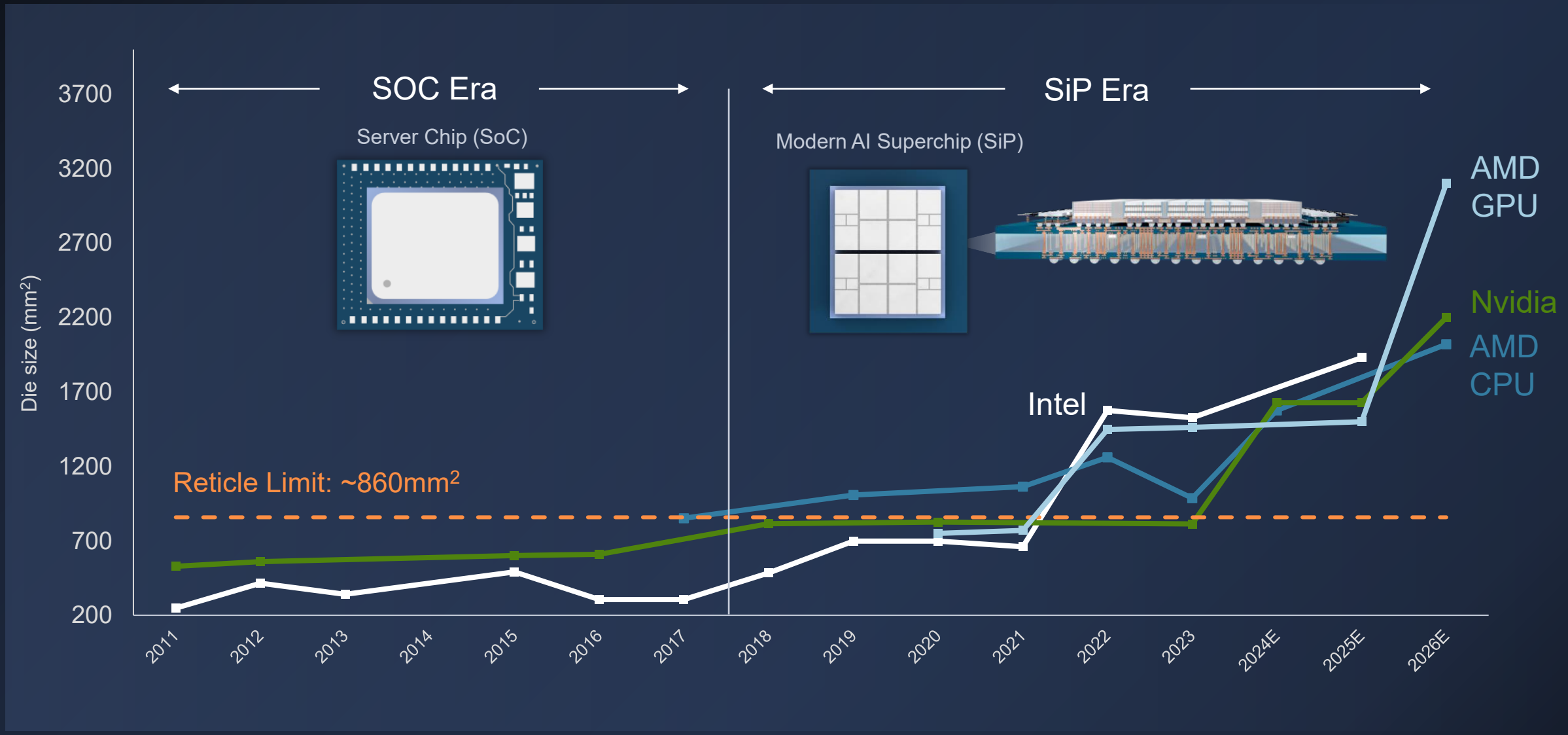


3D model of chip

Stacked copper interconnects

Transistors

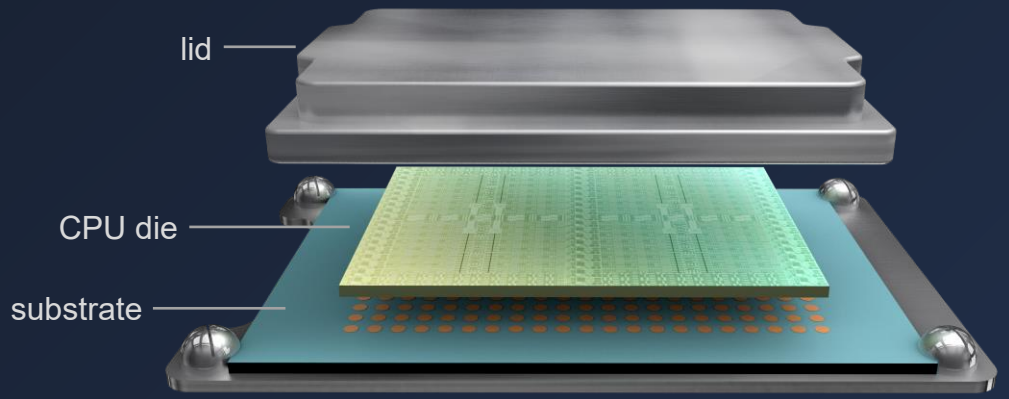
The System-in-a-Package (SiP) Era



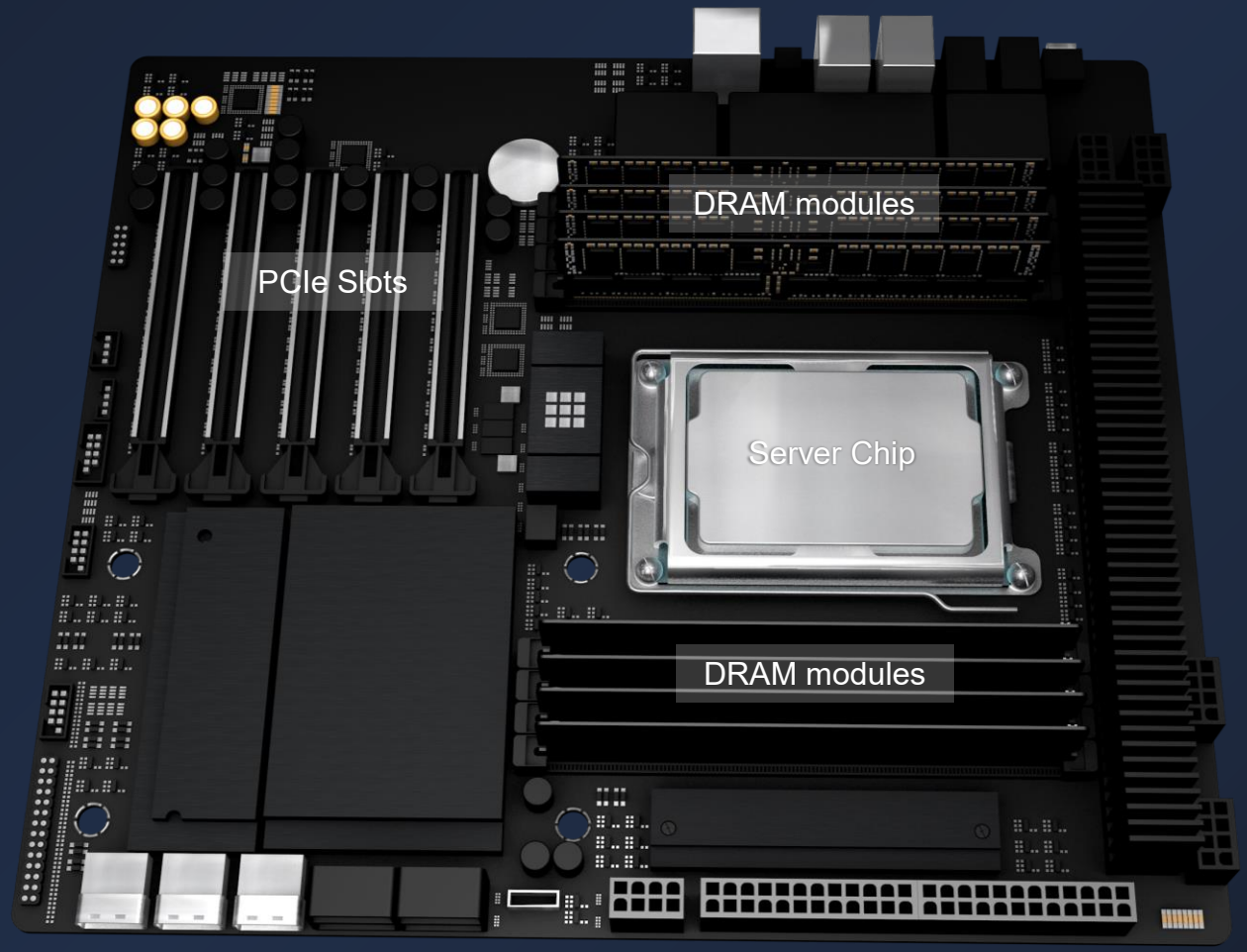
Source: Applied Materials, Evercore ISI Research, Anandtech, wccftech.com, techpowerup.com, Locuza

SoC System Integration

Server Chip



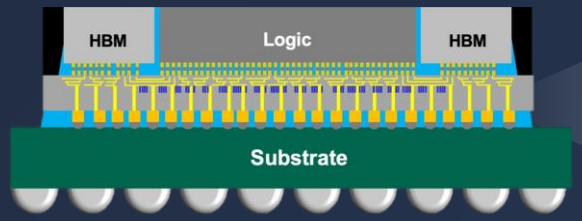
Cross section of Server Chip



Printed Circuit Board (“Motherboard”) with Components

Interposers

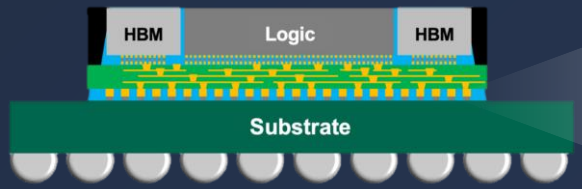
Chip on Wafer on Substrate with Si Interposer (CoWoS-S)



Silicon Interposer

Enables high-density chip interconnects through fine-pitch silicon wiring and TSVs

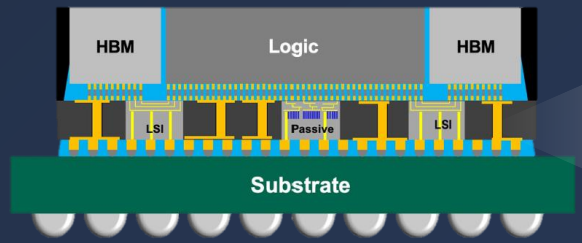
Chip on Wafer on Substrate with RDL Interposer (CoWoS-R)



Epoxy Interposer with Redistribution Layer (RDL)

Uses organic polymer layers for cost-effective die-to-die routing at larger pitch scales

Chip on Wafer on Substrate with RDL Interposer and LSI (CoWoS-L)



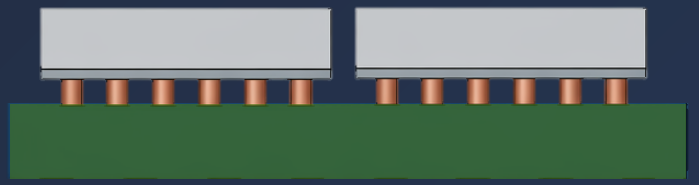
Epoxy Interposer with RDL and Local Silicon Interconnect (LSI)

Embeds silicon bridges in an epoxy RDL substrate for high-bandwidth local die-to-die links

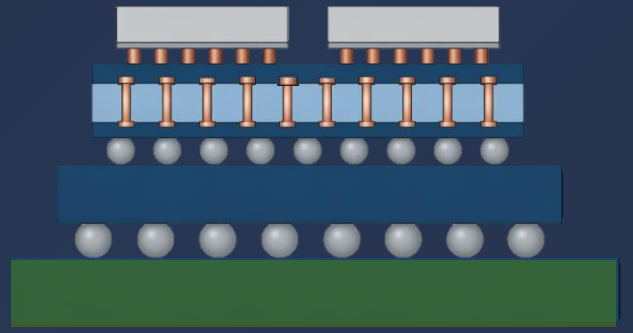
*CoWoS-S, CoWoS-R and CoWoS-L are trademarks of TSMC

Advancing Advanced Packaging

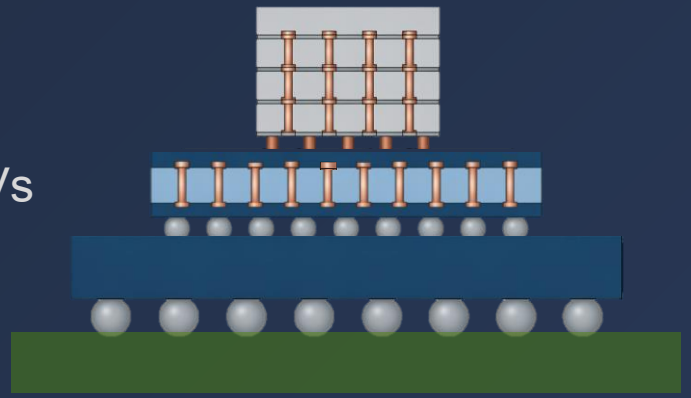
2D
side-by-side chips on PCB



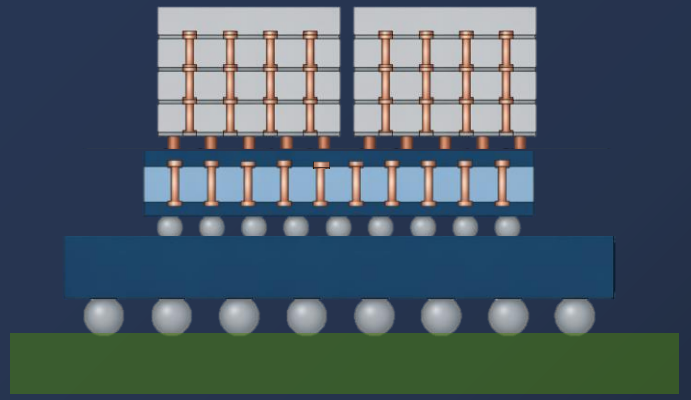
2.5D
dies on silicon interposer



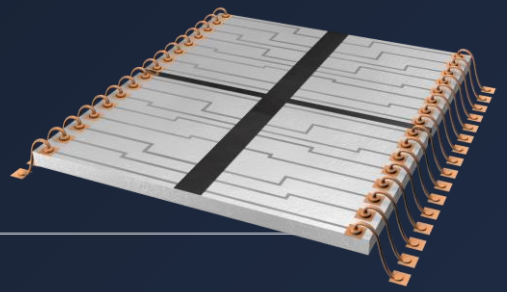
3D
vertical die stacking via TSVs



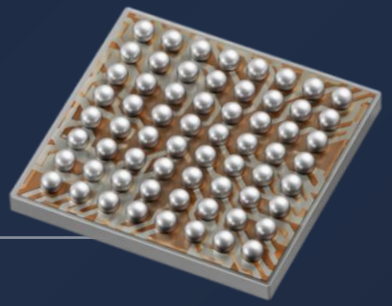
3.5D
3D stacks on 2.5D interposer



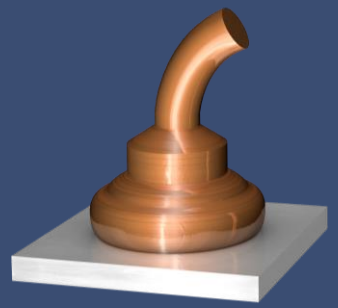
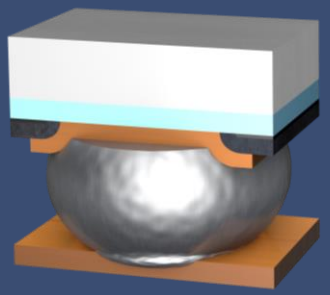
Packaging Interconnects



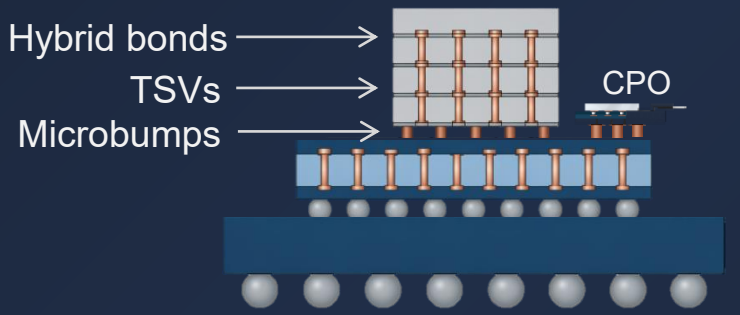
2D Package

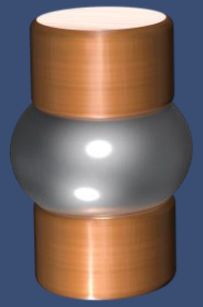
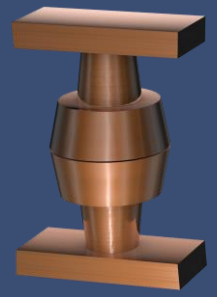
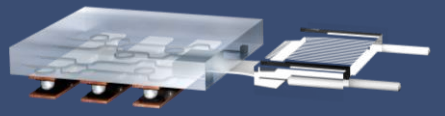


Flip-Chip

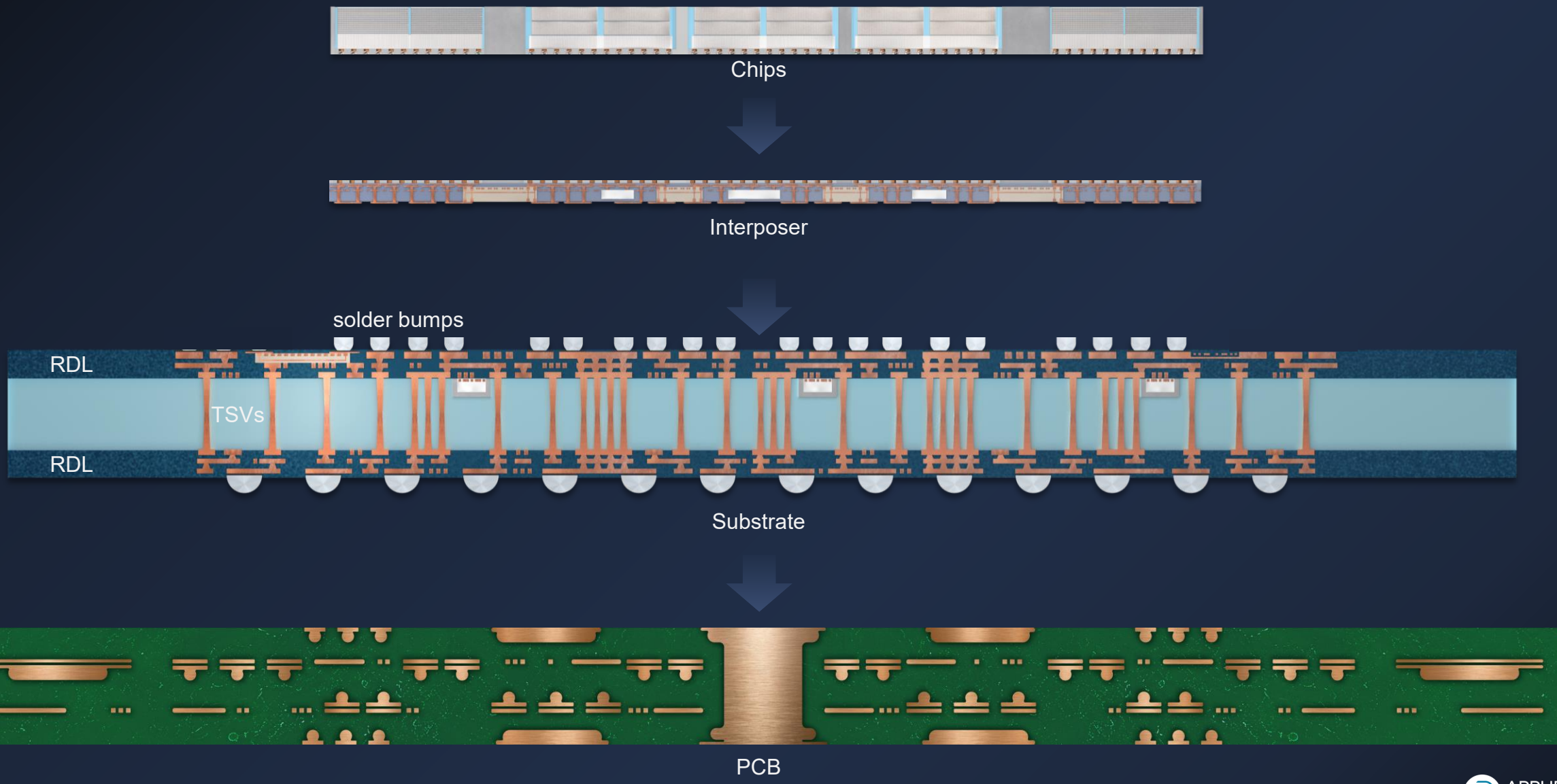
Technique	**Wire Bonds** 	**Solder Bumps** 
Defining Feature	Thin wires arced from chip pads to substrate	Round solder joints connect substrate to PCB
I/O Density	~10/mm²	<100/mm²
Energy per Bit	~10 pJ/bit	~20 pJ/bit

Packaging Interconnects (continued)

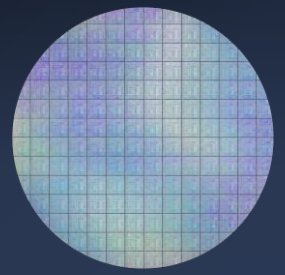


Technique	Microbumps	Through-Silicon Vias (TSVs)	Hybrid Bonds	Co-Packaged Optics (CPO)
				
Defining Feature	Small solder joints connecting chips to interposers	Vertical copper vias etched through silicon die	Direct copper-to-copper fusion between chips	On-package fiber-optic links moving data as light instead of electricity
I/O Density	<1,000/mm²	~10,000/mm²	~1,000,000/mm²	Bandwidth-driven (Tb/s per fiber)
Energy per Bit	~2 pJ/bit	~0.5 pJ/bit	~0.1 pJ/bit	~0.05 pJ/bit

Bridging Chips to Boards: Substrates

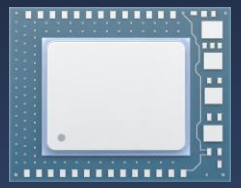


The Path to Super-sized AI Chips: Panel Interposers



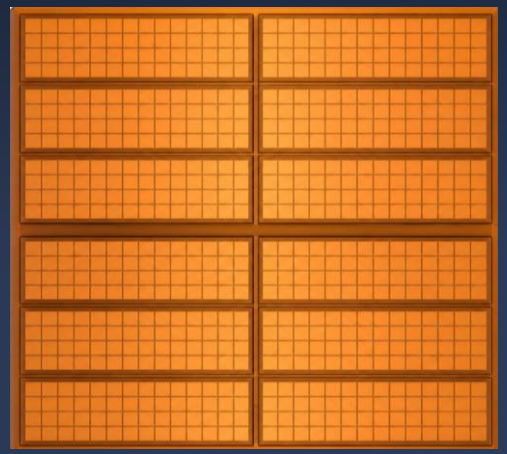
Silicon Wafer Interposers

- 300mm diameter
- Poor area efficiency
  - 5.5x reticle → ~14 interposers
  - 14x reticle → ~5 interposers



2000s Processor

- Package size: 50x50mm^2
- Silicon area: ~100mm^2
- # of dies:1

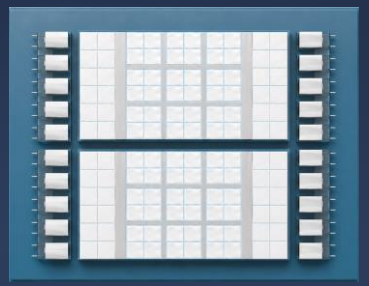


Panel Interposers

Up to 5x larger than wafer

Large interposer houses hundreds of chips

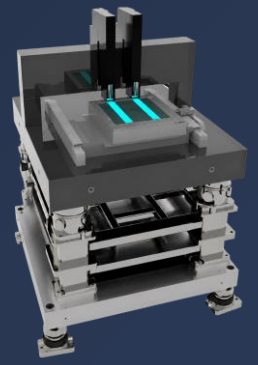
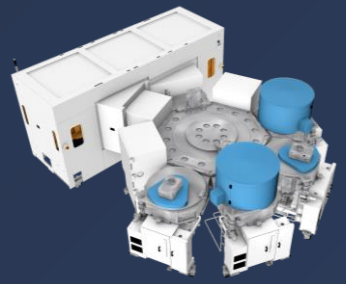
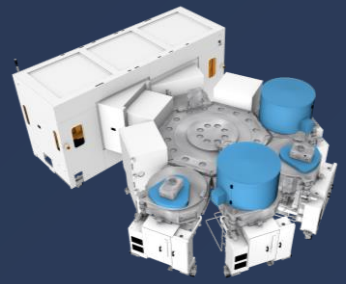
- 310x310mm, 510x515mm, 600x600mm
- Enables 14x-reticle-size interposers
- Materials: epoxy, laminates, glass



Future AI Superchip

- Package size: 9x
- Silicon area: >>600x
- # of dies: 400

Co-optimized Panel Manufacturing Solutions

Lithography	Deposition (PVD)	Deposition (CVD)	Etch	Deposition (ECD)	eBeam Metrology
					
Maskless digital lithography for sub-2-micron patterning	Topaz™ for panels up to 600mm X 600mm	Topaz™ for panels up to 600mm X 600mm	Advanced patterning of panels up to 600mm X 600mm	NEXX Stratus™ P500 for panel copper electroplating	eBeam review technology proven in the LCD industry

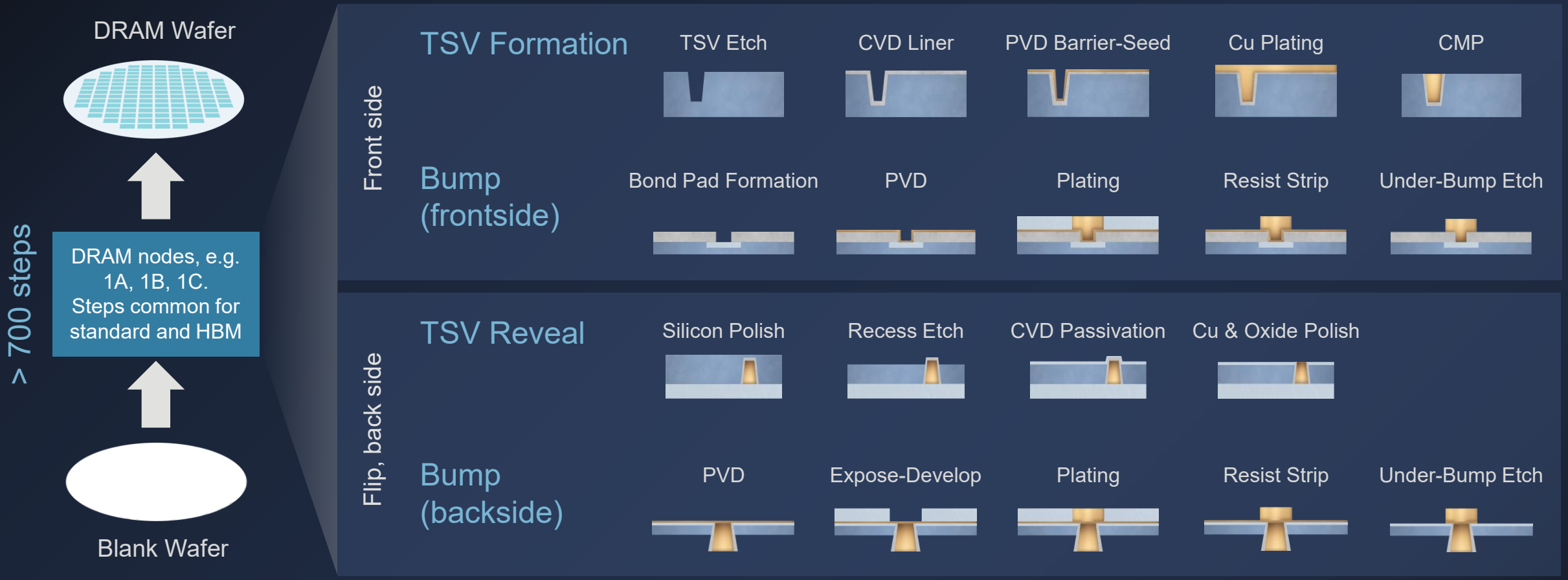
Applied leveraging its front-end process technologies and display expertise for panel packaging

PVD: Physical vapor deposition

CVD: Chemical vapor deposition

ECD: Electrochemical deposition

High-Bandwidth Memory: Incremental Materials Engineering Steps

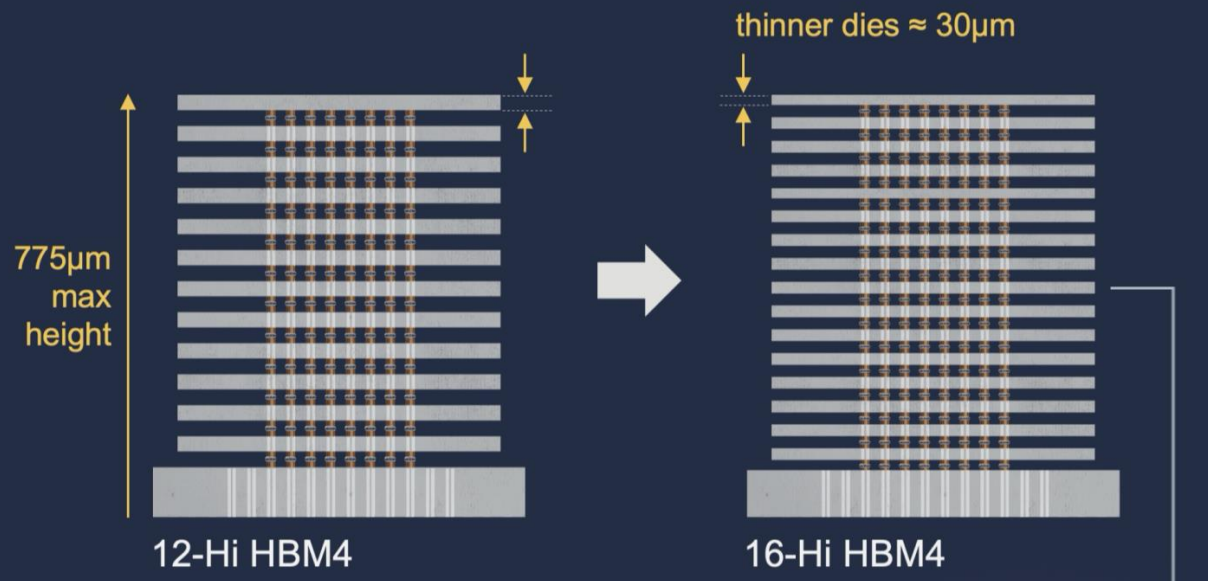


Applied's broad portfolio supports ~3/4 of HBM materials engineering process steps

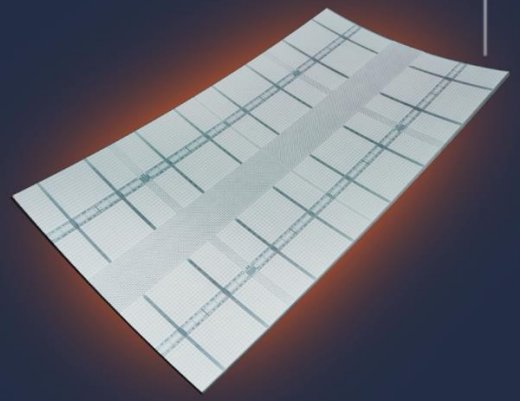
#1 in HBM with SAM share ~50%

Source: Applied Materials analysis

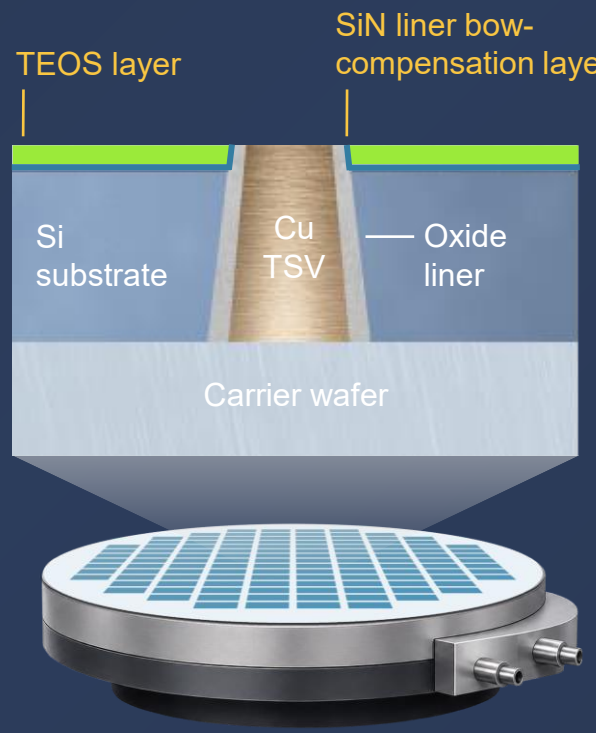
Enabling Thinner DRAM for HBM4 and Beyond



Thinner dies require more bow compensation from TSV films

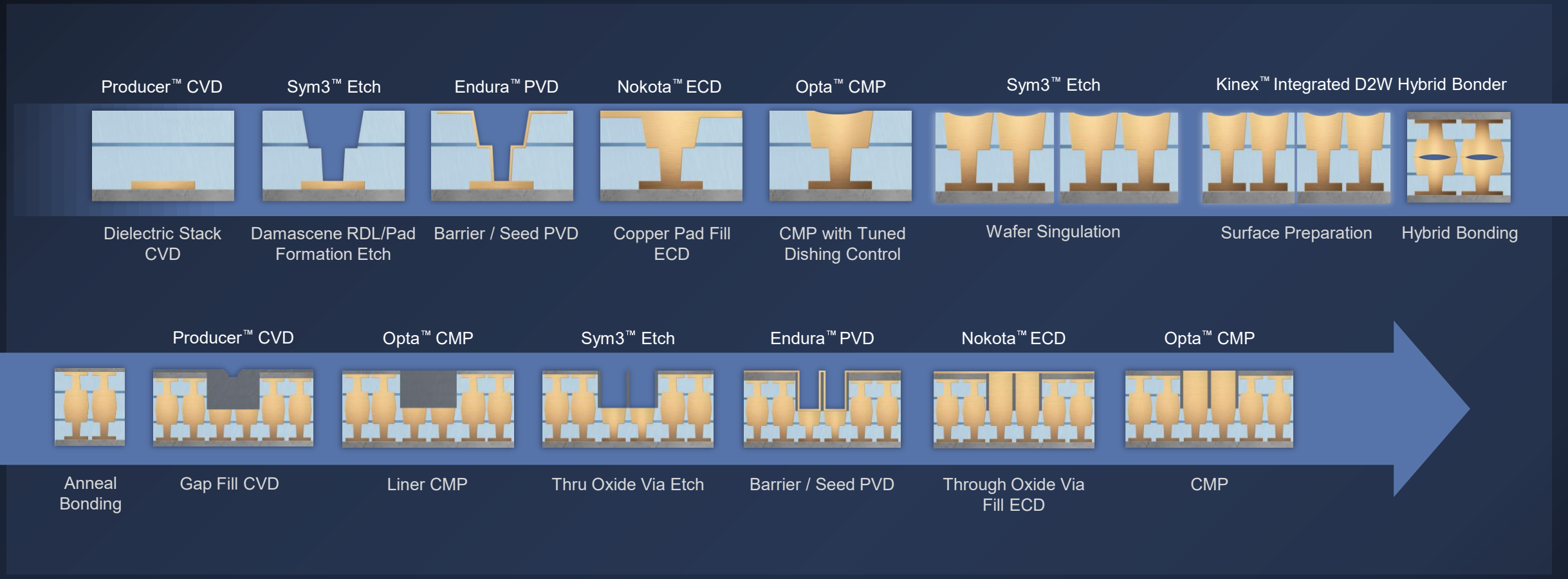


Stress-Engineered Backside TSV Films



Producer™ Avila™ 2 PECVD

Hybrid Bonding Flow



CVD: chemical vapor deposition
RDL: redistribution layer

PVD: physical vapor deposition
ECD: electrochemical deposition

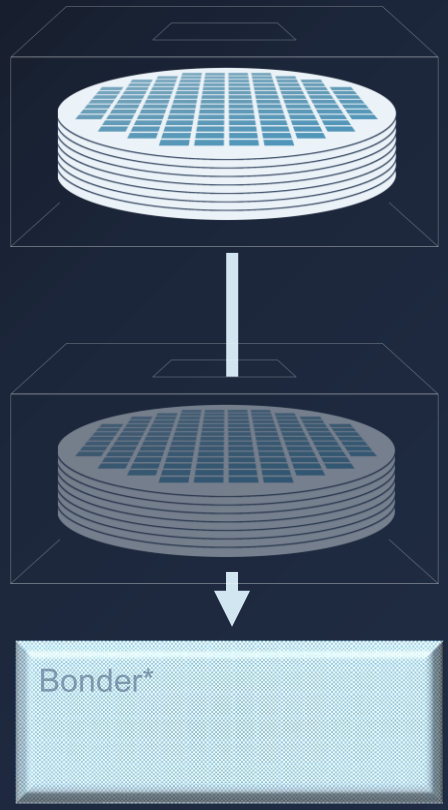
CMP: chemical mechanical polishing

D2W: die-to-wafer
W2W: wafer-to-wafer

Lowering Hybrid Bonding Queue Time to Increase Yield

Stand-Alone Solution

Surface Preparation

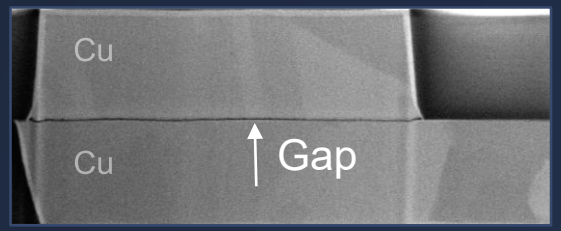


*Bonding 6 chiplets to 25x32 mm target chip
**Foup: 13 wafers, wafer: 897 chiplets

13hrs**

Higher queue time

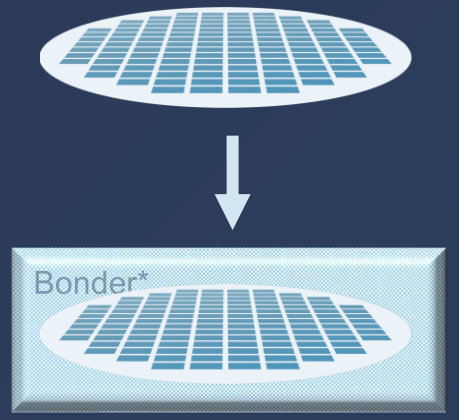
from activation of one wafer
to bonding the last chiplet



Contamination risk

Kinex

Surface Preparation



*Bonding 6 chiplets to 25x32 mm target chip
***1 wafer x 897 chiplets/wafer

1hr***

Lower queue time

improves bond quality

Improved adhesion

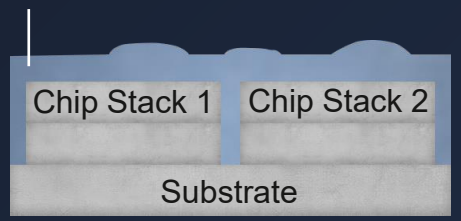
Improved yield

Kinex™ Integrated Die-to-Wafer Hybrid Bonding System

Advanced Packaging CMP Innovations

Copper Fill with thickness variation

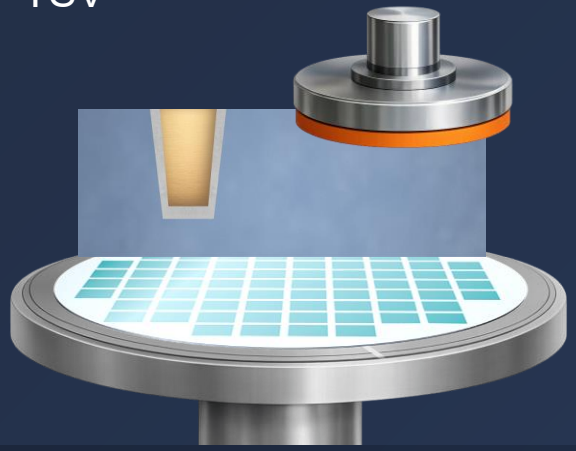
Oxide Dielectric with thickness variation

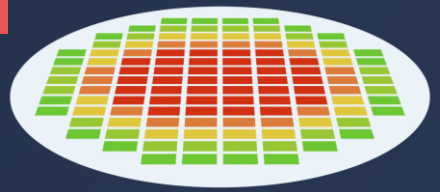


Chemical Mechanical Planarization (CMP)

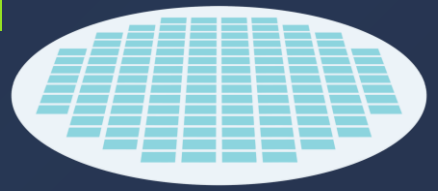
Opta™ Quad CMP

TSV



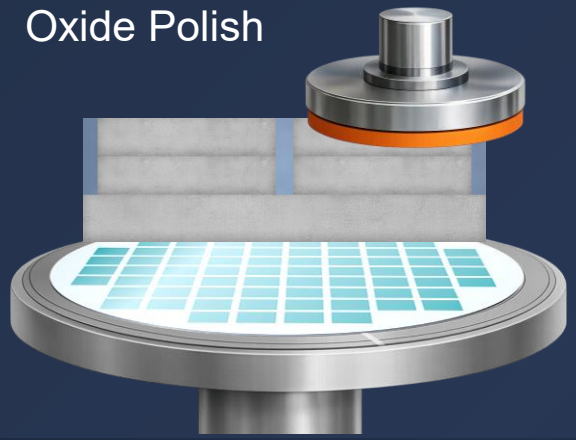


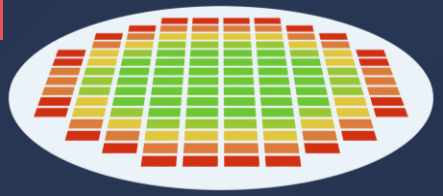
High wafer-within-wafer total thickness variation with conventional CMP



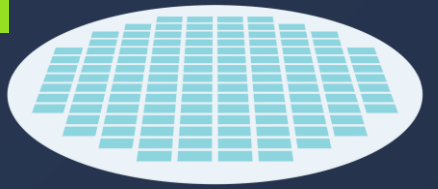
Low wafer-within-wafer total thickness variation

Oxide Polish





Poor edge uniformity with conventional CMP



Edge profile control corrects thickness variation to improve die yield

APPLIED MATERIALS

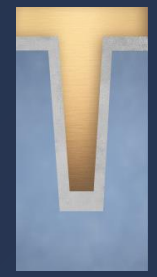
Advanced Packaging ECD Innovations

TSV Barrier / Seed PVD

Cu Pad TSV Fill

Conventional ECD struggles to deliver chemistry in high-aspect-ratio structures, resulting in voids and defects

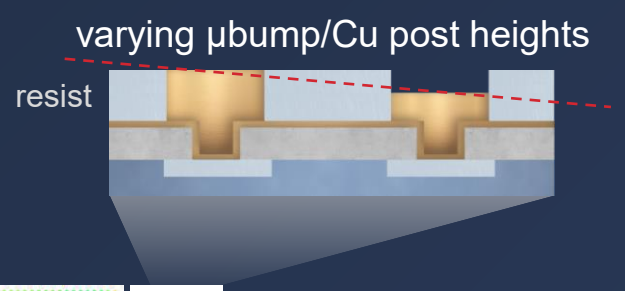
Nokota™ Vmax 2 ECD

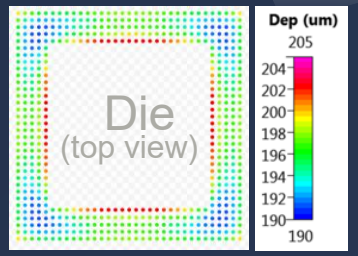


Nokota enables void- and defect-free TSV fill for dimensions as small as 3 microns

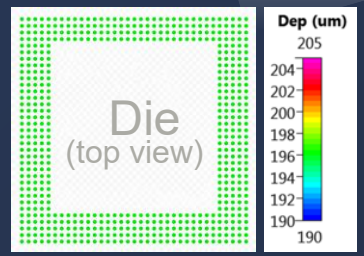
µbump Barrier / Seed PVD

µbump and Cu Post Deposition



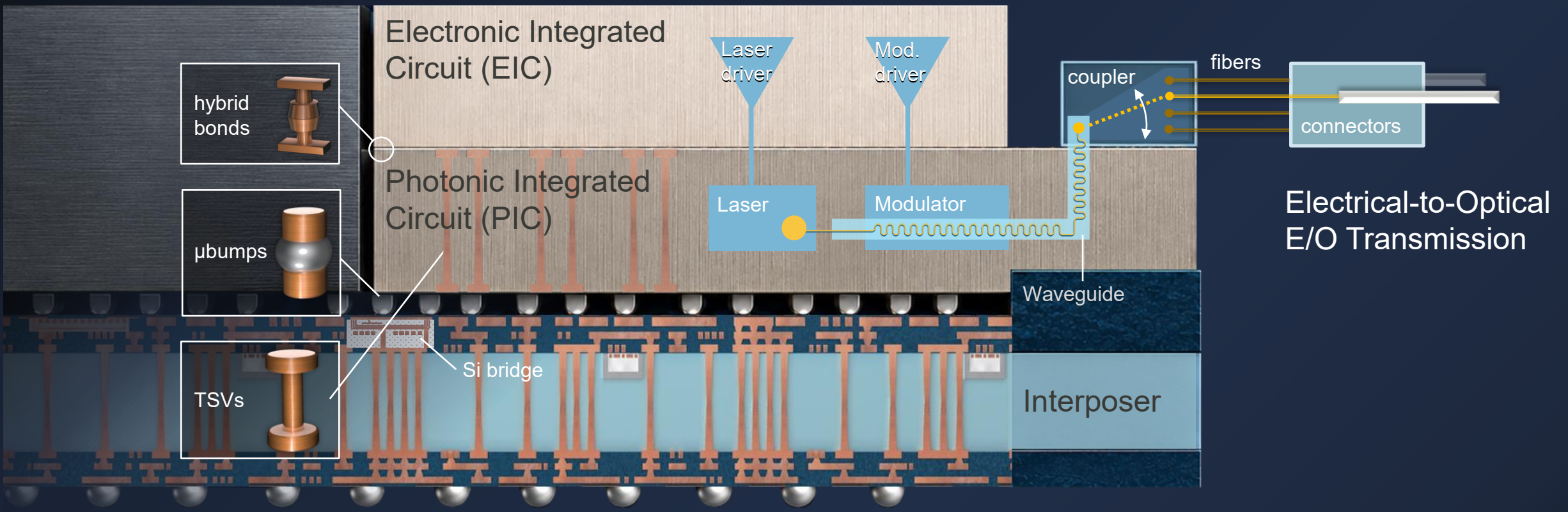


High wafer pattern variations result in uneven Cu deposition around die edges in conventional ECD



Adaptive pattern tuning enables even metal deposition and higher coplanarity

Advanced Packaging Enables Co-Packaged Optics



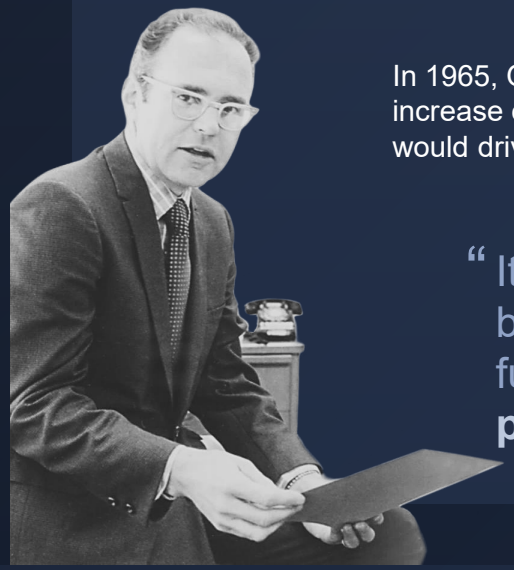
Electrical-to-Optical E/O Transmission

Co-Packaged Optics (CPO) overcome the physical bottlenecks of traditional data networking – bandwidth limits, power consumption and signal degradation – by bringing optical components as close as possible to electronic chips (ASICs, EICs, etc.)

Applied Ventures, LLC

Semiconductor Systems

More Than Moore



In 1965, Gordon Moore predicted both the exponential increase of transistors on a chip, and conditions that would drive *the disaggregation of the system-on-chip*.

> "It may prove to be more economical to build **large systems** out of smaller functions, which are **separately packaged and interconnected**"

	Without Advanced Packaging	**With** Advanced Packaging
# of Transistors	200 Billion	1.6 Trillion
Silicon Content	1x	4x

https://archive.computerhistory.org/resources/access/text/2017/03/102770822-05-01-acc.pdf

MASTER CLASS June 25, 2026

Lior Engel

Corporate Vice President
Imaging and Process Control Group

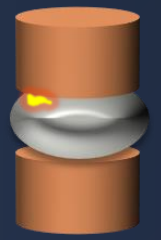
APPLIED MATERIALS

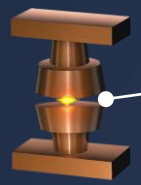
Advanced Packaging Needs Advanced Process Control

Traditional Packaging Served by Optical

Emerging Advanced Packaging Needs

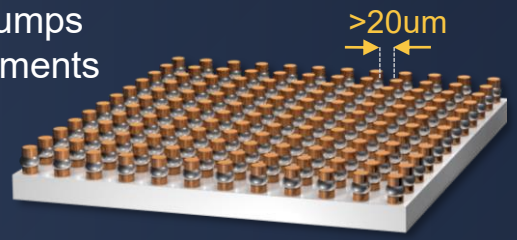
Particle on bump

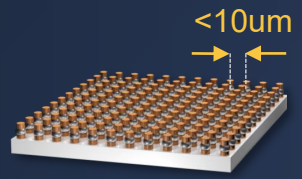




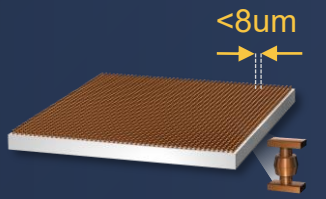
Small particles are becoming yield killers

Solder bumps measurements



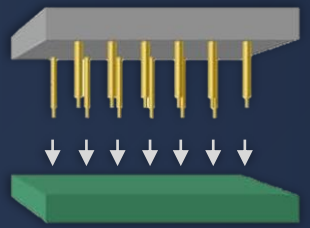


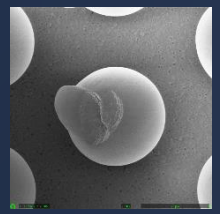
Microbumps



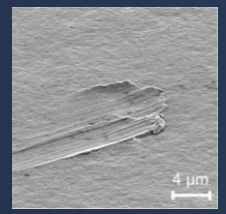
Hybrid Bonds

Physical probers





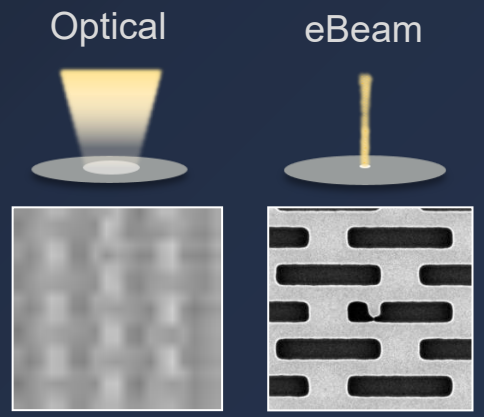
Bump damage



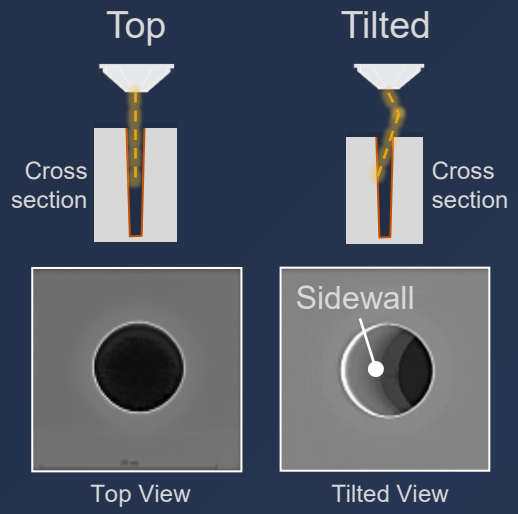
Cu pad damage

eBeam Benefits in Advanced Packaging

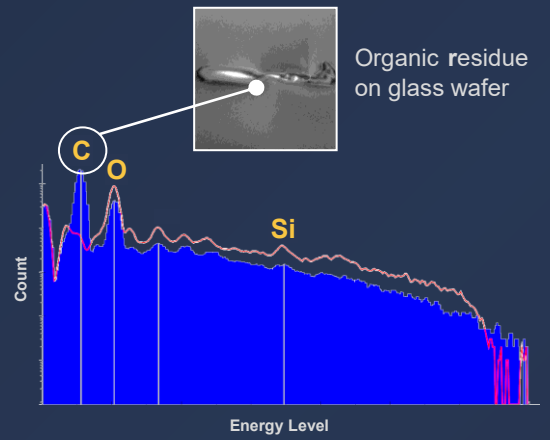
Higher Resolution



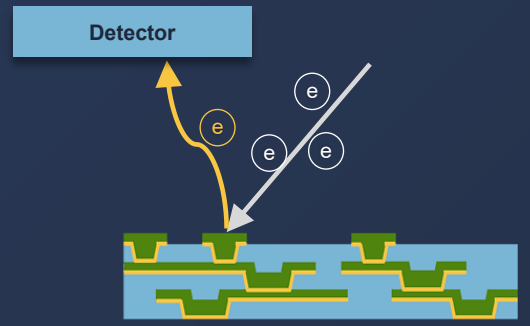
Tilted / 3D Imaging



Material Identification



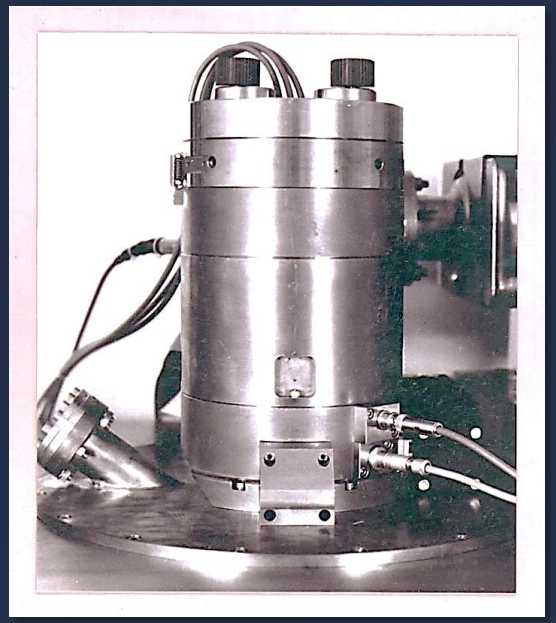
Non-Contact Electrical Test



eBeam Leadership

1980s

eBeam Innovation Begins



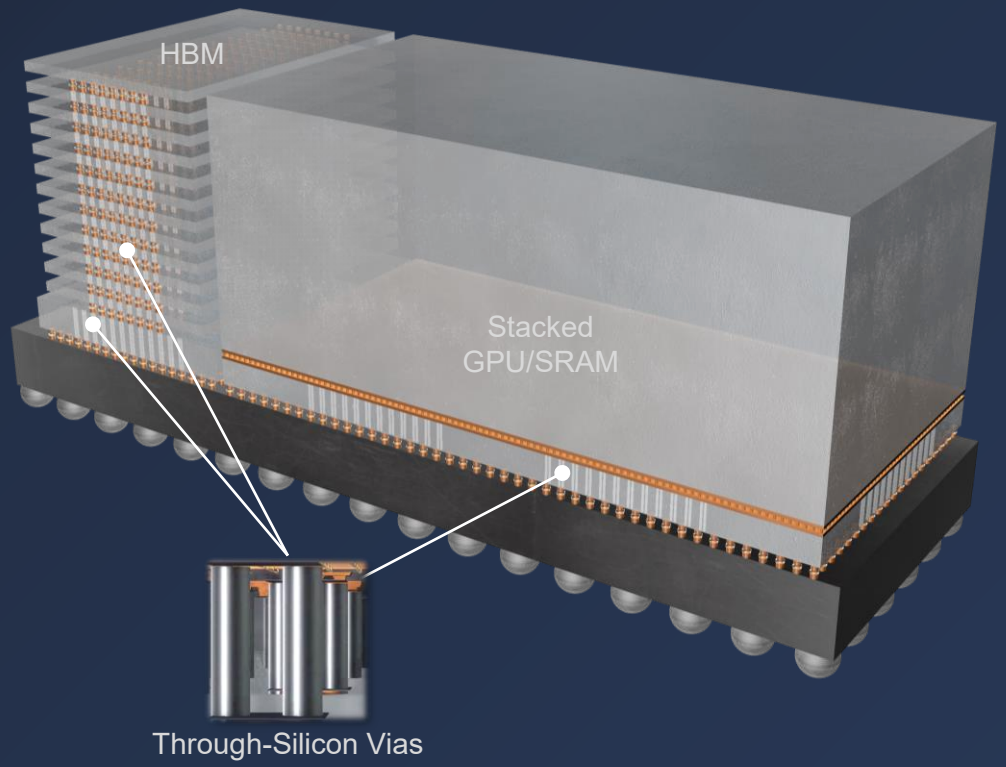
Today

#1 Market Position

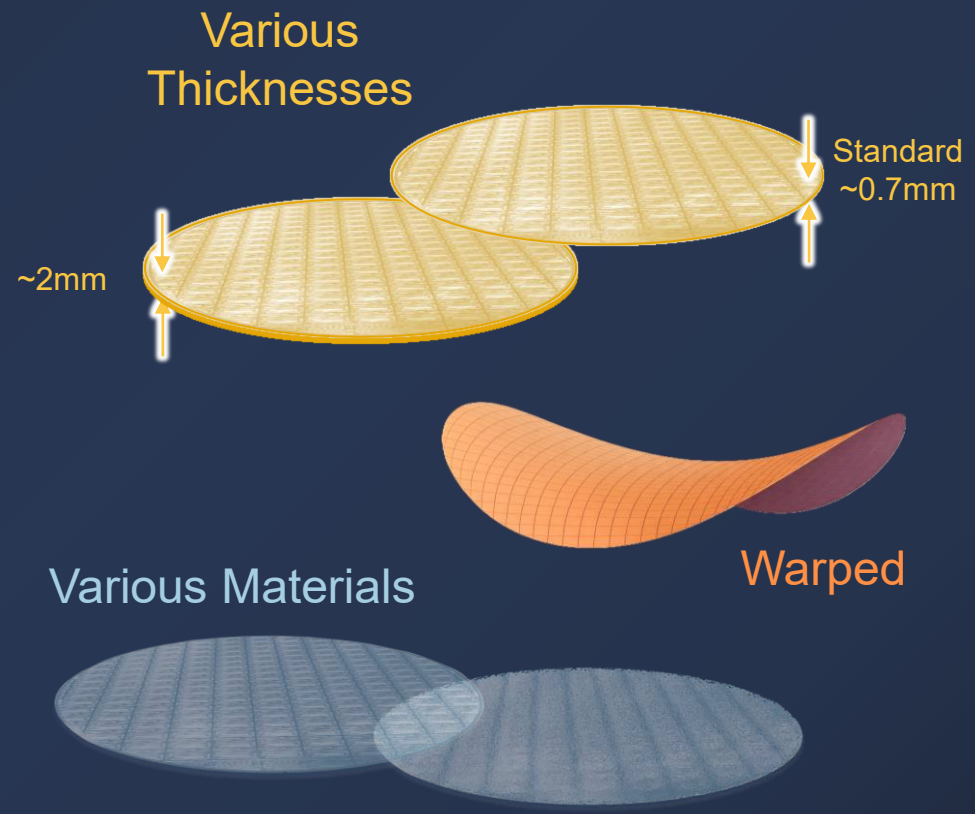
40+ Years of eBeam Leadership

eBeam Enabling Process Control in Advanced Packaging

High-Density 3D Architectures



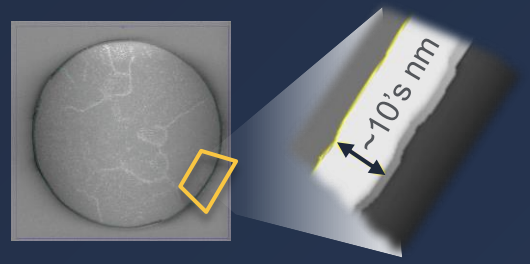
Diverse Substrates and Warpage Challenges



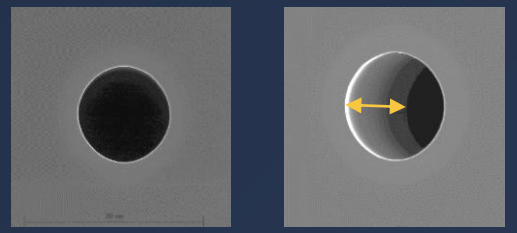
CD Metrology – VeritySEM™ 7AP

Metrology

Hybrid Bonding Pads
Diameter, barrier seed roughness

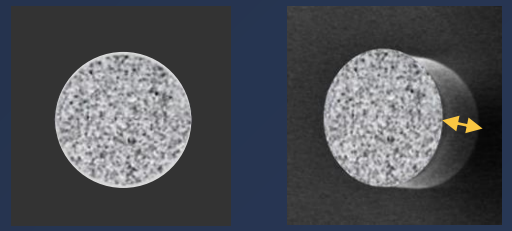


TSV
Top/Bottom CD, slant, sidewall



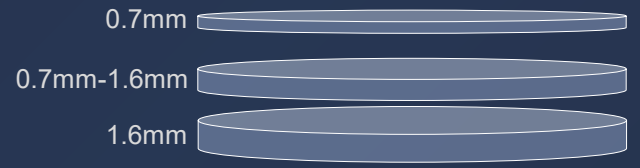
Unique tilted beam capability

Microbump
Diameter, height, cross-wafer trends

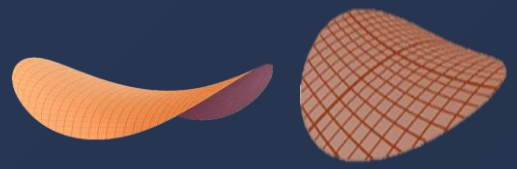


Wafer Handling Capability

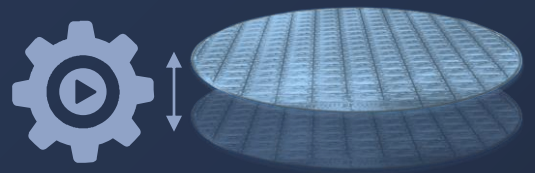
Varied Thicknesses



Warpage

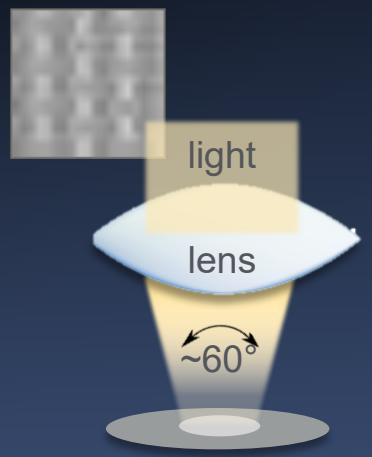


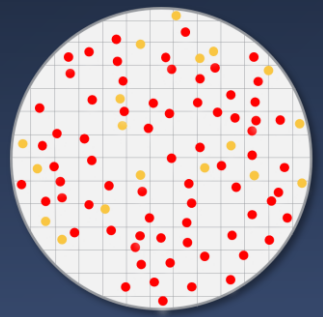
Fully Automated Tool Configuration

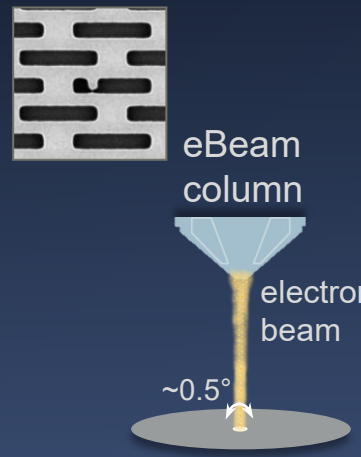


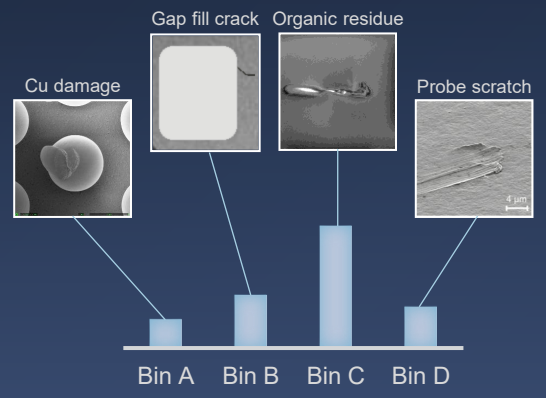
VeritySEM™ 7AP CD Metrology

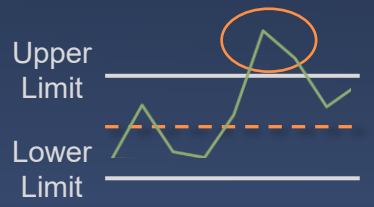
Optical Inspection and Defect Review Flow











Optical Inspection | **Defect Map** | **eBeam Defect Review** | **Defect Binning** | **Control Chart**

SEMVision™ G7AP Defect Analysis

MASTER CLASS June 25, 2026

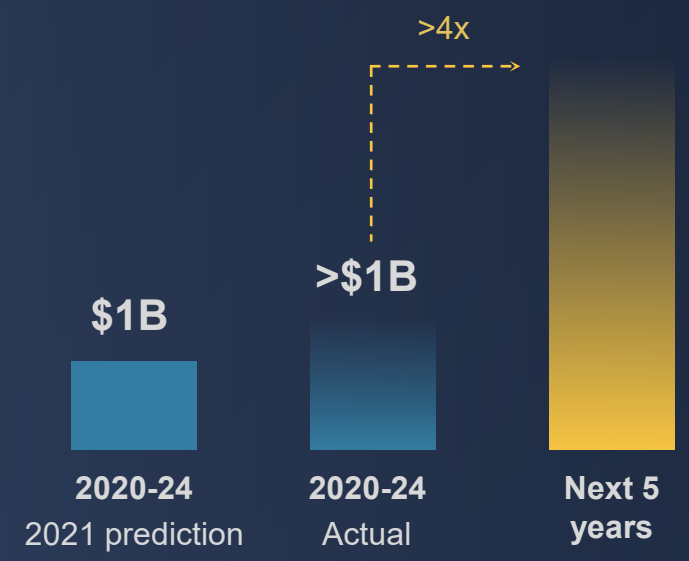
Kevin Moraes, Ph.D.

Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

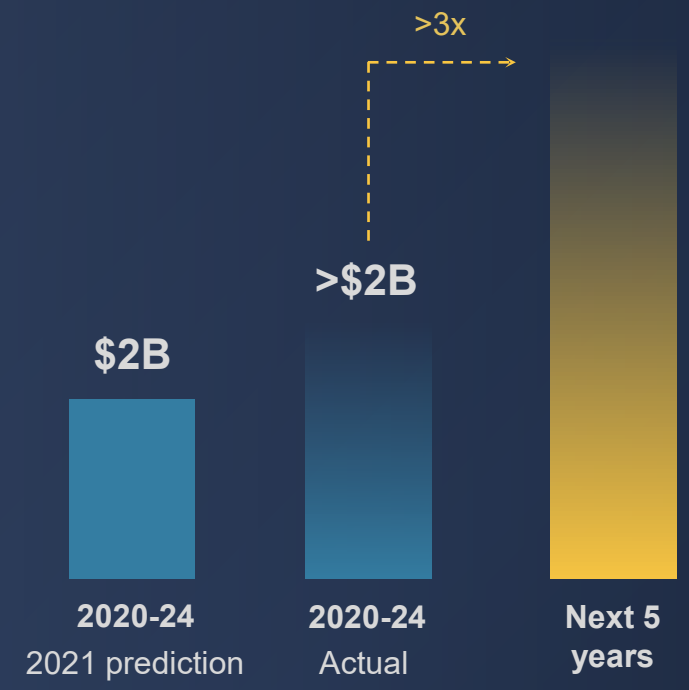
APPLIED MATERIALS

Exceeding Previous Growth Expectations

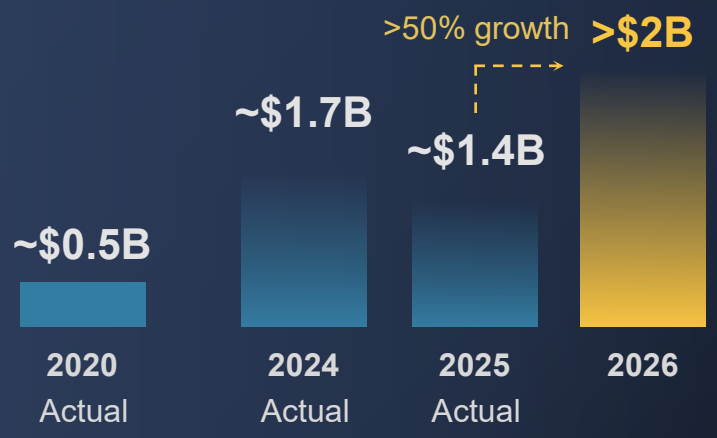
Growing by Enabling the Capacitor Roadmap



Leadership in Periphery Transistor and Interconnect Scaling



Well Positioned for Growth in Advanced Packaging



APPLIED MATERIALS

EPIC CENTER GAINING MOMENTUM

FOUNDING PARTNERS

- Micron
- Samsung
- SK hynix
- TSMC

INNOVATION PARTNERS

- Advantest
- SCREEN
- Broadcom

RESEARCH PARTNERS

- ASU
- RPI
- Stanford

Key Takeaways

Demand is accelerating and broadening with **incremental AI drivers**	Leading-edge foundry-logic (F/L), DRAM, and advanced packaging are most critical to enabling improvements in tokens per second per watt and are driving the vast majority of WFE investment growth.
Applied has **built process equipment leadership** in leading-edge F/L, DRAM and advanced packaging, and expects to **extend leadership** as SAM and share opportunities increase with **new inflections**	Applied's DRAM leadership drives five key inflections to scale density, bandwidth, and speed: EUV-driven $6F^2$ scaling, CMOS-bonded arrays, $4F^2$ vertical transistors, 3D DRAM with increased emphasis on conductor materials engineering versus NAND, and more logic technologies through advanced periphery transistors and wiring.
	Applied's on-chip leadership extends to advanced packaging for key inflections: HBM, hybrid bonding, co-packaged optics and panels. Larger AI accelerator packages are accelerating the move to panel—which can expand usable interposer area by >7x versus 300 mm wafers—and Applied has built the industry's largest panel portfolio.
	As packaging complexity and defect sensitivity increase, Applied's industry-leading eBeam process control is critical to enabling high-yield manufacturing for advanced 2.5D, 3D and 3.5D systems.
EPIC extends Applied's inflection-focused innovation strategy	Industry co-innovation and customer roadmap visibility enable earlier design-in and greater value capture at future technology inflections.

APPLIED MATERIALS™

Material Innovation