



NEWS RELEASE

Applied Materials Introduces New Technologies and Capabilities for Accelerating the Semiconductor Industry's Heterogeneous Integration Roadmap

- *New advanced software modeling and simulation for die-to-wafer hybrid bonding at Applied's Advanced Packaging Development Center speeds customer time to market*
- *Enters into joint development agreement with EV Group for co-optimized wafer-to-wafer hybrid bonding solutions*
- *Enables larger, higher quality substrates for advanced packaging through the recent acquisition of Tango Systems, a leader in panel-level processing*
- *Provides customer access to large-area yield management solutions and other technologies from its Display business*

SANTA CLARA, Calif., Sept. 8, 2021 – Applied Materials, Inc. today introduced new technologies and capabilities designed to help its customers accelerate their technology roadmaps for heterogeneous chip design and integration.

Applied is combining its leadership technologies in advanced packaging and large-area substrates with industry collaborations to speed the availability of solutions that deliver simultaneous improvements in power, performance, area, cost and time to market (PPACt™).

Heterogeneous integration brings new kinds of design and manufacturing flexibility to semiconductor and system companies by allowing chips of various technologies, functions and sizes to be integrated in one package. Applied is already the largest supplier of advanced packaging technologies with optimized products spanning etch, physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, surface treatments and annealing. Applied's Advanced Packaging Development Center in Singapore houses the industry's broadest portfolio of products that enable the foundational building blocks of heterogeneous integration, including advanced bump and micro-bump, fine-line redistribution layer (RDL), TSV and hybrid bonding.

"Applied's industry-leading portfolio of advanced packaging solutions gives customers the broadest selection of enabling technologies for heterogeneous integration," said Nirmalya Maity, Corporate Vice President of Advanced Packaging at Applied Materials. "Through technology co-optimization and collaboration with others in the industry, we are building an ecosystem that can accelerate our customers' PPACt roadmaps and create exciting new growth opportunities for Applied."

Today, Applied is unveiling innovations in three areas critical to advanced packaging for heterogeneous integration: die-to-wafer hybrid bonding, wafer-to-wafer bonding and advanced substrates.

Accelerating Die-to-Wafer Hybrid Bonding

Die-to-wafer hybrid bonding uses direct, copper-to-copper interconnects to increase I/O density and shorten the wiring length between chiplets to improve overall performance, power and cost. To accelerate development of this technology, Applied is adding advanced software modeling and simulation to its Advanced Packaging Development Center. These capabilities allow various parameters such as material selection and packaging architecture to be evaluated and optimized prior to hardware development to significantly accelerate learning cycles and speed time to market for customers. This builds upon the joint development agreement [announced in October 2020](#) between Applied and BE Semiconductor Industries N.V. (Besi) to develop the industry's first complete and proven equipment solution for die-based hybrid bonding.

"Our joint development program with Applied Materials has greatly enhanced our combined understanding of the co-optimized equipment solutions necessary for customers to utilize complex hybrid bonding processes in wafer level production environments," said Ruurd Boomsma, Besi's Chief Technology Officer. "In a very short time, the Besi and Applied teams have made excellent progress working together at the Hybrid Bonding Center of Excellence in Singapore to process customer materials and accelerate development of advanced heterogeneous integration technologies."

Developing Co-optimized Solutions for Wafer-to-Wafer Hybrid Bonding

Wafer-to-wafer bonding enables chipmakers to build certain chip structures on one wafer and others on a second wafer and then bond the wafers to create complete devices. In order to achieve high performance and yield, the quality of the front-end processing steps is critical as is the precise uniformity and alignment of the wafers as they are being bonded. Applied today announced a joint development agreement with EV Group (EVG) to develop co-optimized solutions for wafer-to-wafer bonding. The collaboration brings together Applied's semiconductor process expertise in deposition, planarization, implant, metrology and inspection with EVG's leadership in wafer bonding, wafer pre-treatment and activation, as well as alignment and bond overlay metrology.

"Semiconductor innovation is increasingly being fueled by 3D integration and engineered materials, which drives greater demand for wafer-to-wafer hybrid bonding. Optimizing this critical process for new applications requires an in-depth understanding of integration issues both up and down the process chain," said Dr. Thomas Uhrmann, Business Development Director at EVG. "Industry collaborations like the one that we have with Applied Materials allow us to share data and learn from different areas of strength among process equipment companies, which enables us to co-optimize our solutions and better solve our customers' emerging and critical manufacturing challenges."

"Through collaborations with industry partners including Besi and EVG, Applied Materials is providing our customers the capabilities and expertise they need to accelerate development and adoption of hybrid bonding technologies, both die-to-wafer and wafer-to-wafer," said Vincent DiCaprio, Managing Director of Business Development for Advanced Packaging at Applied Materials. "Applied looks forward to building further engagements in the ecosystem as chipmakers increasingly use heterogeneous design techniques to drive their PPACt roadmaps."

Larger, More Advanced Substrates Deliver PPAC Benefits

The need for more advanced substrates is increasing as chipmakers squeeze greater numbers of chips into sophisticated 2.5D and 3D package designs. To enable larger package sizes with greater interconnect density, Applied is using state-of-the-art panel-level processing technology from its recent acquisition of Tango Systems. Panel-size substrates, which can measure 500mm x 500mm or larger, can accommodate a greater number of packages compared to wafer-size formats, thereby providing a cost benefit in addition to better power, performance and area.

As its customers adopt these larger panel sizes, Applied is providing them with access to large-area materials engineering technologies from its Display Group, including deposition, eBeam testing, SEM review and metrology, and focused ion beam for defect analysis.

Additional details on Applied's packaging technologies will be discussed at the company's [2021 ICAPS and Packaging Master Class](#) being held today.

About Applied Materials

Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible a better future. Learn more at www.appliedmaterials.com.

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