



NEWS RELEASE

Applied Materials' New Ioniq™ PVD System Solves Wiring Resistance Challenges of 2D Scaling

SANTA CLARA, Calif., May 26, 2022 – Applied Materials, Inc. today introduced a new system that re-engineers the deposition of transistor wiring to significantly reduce electrical resistance, which has become a critical bottleneck to further improvements in chip performance and power.

Chipmakers are using advances in lithography to shrink chips to the 3nm node and beyond. Unfortunately, as the wires become thinner, the electrical resistance increases exponentially, and this reduces chip performance and increases power consumption. If left unchecked, the wiring resistance can fully negate the benefits of smaller transistors.

Chip wiring is deposited into trenches and vias that are etched into a dielectric material. In the conventional approach, the wiring is deposited using a metal stack that typically includes a barrier layer to prevent the metal from mixing with the dielectric; a liner layer to promote adhesion; a seed layer to facilitate metal fill; and a conductive metal like tungsten or cobalt for the transistor contacts and copper for the interconnect wires. The barriers and liners don't scale well, so as the trenches and vias shrink, the proportion of space available for conductive metals is reduced; and the smaller the wiring, the higher the electrical resistance.

Applied Endura® Ioniq™ PVD System

The [Ioniq PVD system](#) is an Integrated Materials Solution™ (IMS™) that includes surface preparation along with PVD and CVD processes in a single, high-vacuum system. Ioniq PVD enables chipmakers to replace the high-resistance liner and barrier layers, typically made of titanium nitride, with a pure, low-resistance PVD tungsten film which is then combined with CVD tungsten to create a pure tungsten metal contact. The solution solves the resistance challenges and enables 2D scaling to continue to the 3nm node and beyond.

“Applied’s latest breakthrough in solving electrical resistance is a great example of how materials engineering innovations enable 2D scaling to continue,” said Dr. Prabu Raja, Senior Vice President and General Manager of the Semiconductor Products Group at Applied Materials. “The innovative Ioniq PVD system removes a significant bottleneck to extracting performance from transistors, allowing them to operate faster and with lower power losses. As chip complexity increases, the ability to integrate multiple processes in high vacuum becomes critical to creating advancements in wiring that enable customers to achieve their performance and power goals.”

The Endura Ioniq PVD system has been selected by multiple leading customers worldwide. Additional information about the system and other Applied Materials solutions for solving critical wiring and interconnect challenges will be discussed at the company’s [“New Ways to Wire and Integrate Chips”](#) Master Class being held later today.

About Applied Materials

Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible a better future. Learn more at www.appliedmaterials.com.

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