ICAPS AND PACKAGING MASTER CLASS

September 8, 2021

Forward-Looking Statements and Other Information

Today's presentations contain forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, our business outlook for the fourth quarter of fiscal 2021 and beyond, the impact of the ongoing COVID-19 pandemic and responses thereto on our operations and financial results, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; global economic and industry conditions; the effects of regional or global health epidemics, including the severity and duration of the ongoing COVID-19 pandemic; global trade issues and changes in trade and export license policies, including rules and interpretations promulgated by U.S. Department of Commerce expanding export license requirements for certain products sold to certain entities in China; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; acquisitions, investments and divestitures; changes in income tax laws; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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2021 Master Classes

WELCOME

Michael Sullivan
Corporate Vice President
Head of Investor Relations

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UPCOMING INVESTOR EVENTS

MASTER CLASSES

April 6	May 5	June 16	September 8	October 18*
2021 Investor Meeting	Memory	Logic	ICAPS & Advanced Packaging	Process Control & AppliedPRO™

* Projected Date

AGENDA

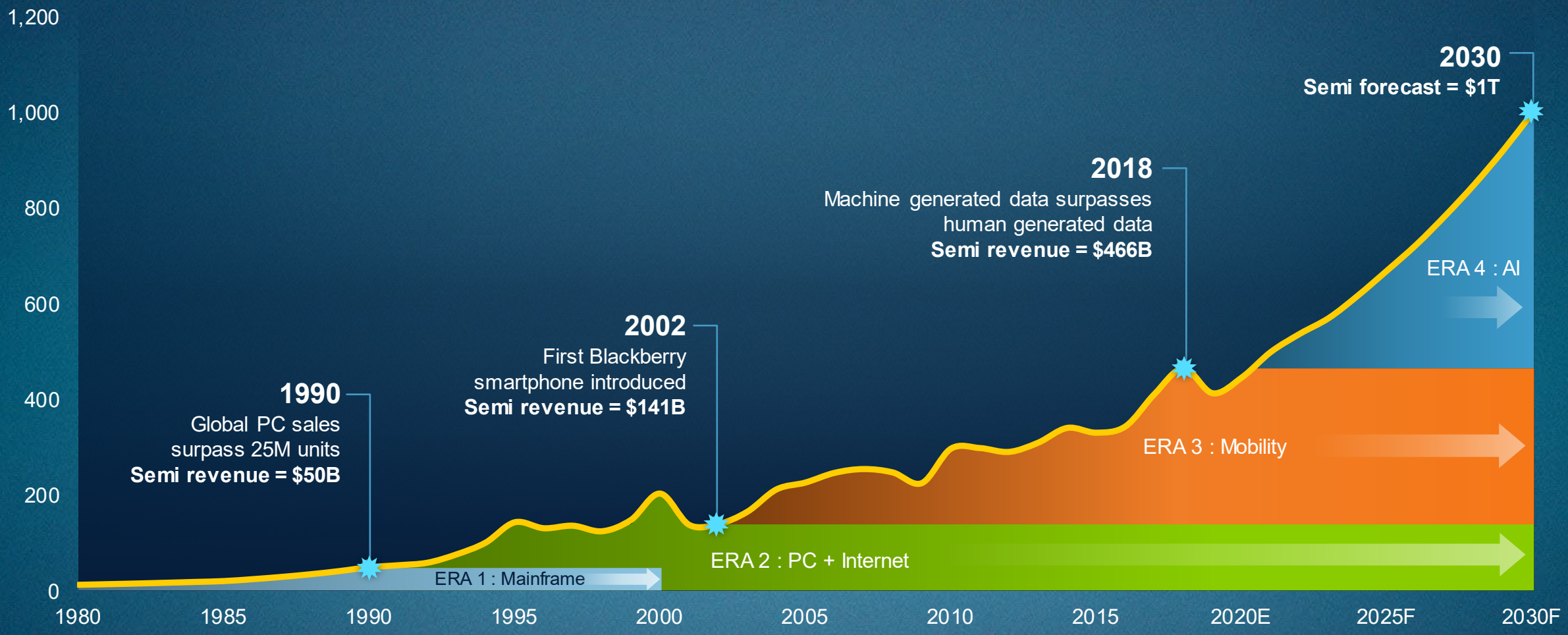
9:00	**PART 1**	HOST: Mike Sullivan Foundry-Logic Growth Thesis Fireside Chat | Tom Caulfield, Ph.D., GlobalFoundries
9:15	**PART 2**	HOST: Sundar Ramamurthy, Ph.D. ICAPS and Advanced Packaging Introduction ICAPS | Michael Chudzik, Ph.D. Packaging | Nirmalya Maity, Ph.D.
9:55	**PART 3**	HOST: Sundar Ramamurthy, Ph.D. ICAPS and Advanced Packaging Growth Opportunities
10:05	**Q&A**	Sundar, Nirmalya, Mike

TAKEAWAY
Messages

1. ICAPS markets fuel data generation at the edge and demand for leading-edge logic and memory in the cloud
2. Advanced packaging enables the PPACt™ benefits associated with Moore's Law to continue
3. Applied's unique portfolio breadth enables outperformance in ICAPS and advanced packaging

* Non-GAAP adjusted EPS

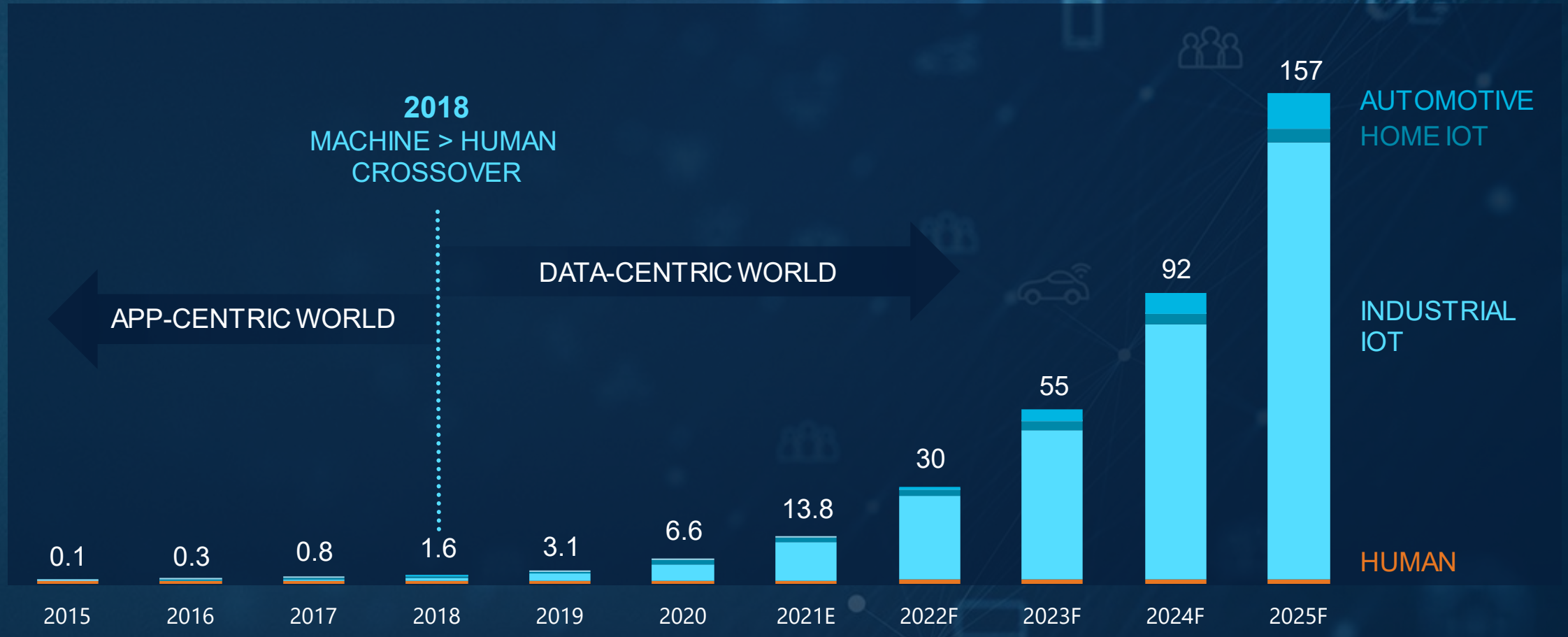
Semiconductor Industry Revenue ($B)



AI ERA WILL BE BIGGEST AGE OF COMPUTING

Source: SEMI, VLSI, Applied Materials

Data Generation By Category (ZB)



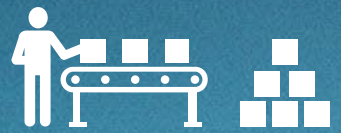
SEMI GROWTH NO LONGER LIMITED BY HUMAN CONSUMPTION

Source: Applied Materials

INDUSTRY 1.0

Mechanization, steam power, weaving loom

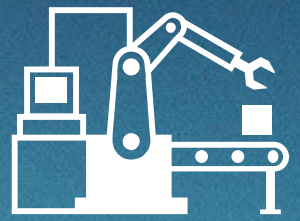
1784



INDUSTRY 2.0

Mass production, assembly line, electrical energy

1870



INDUSTRY 3.0

Automation, computers and electronics

1969

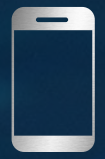
INDUSTRY 4.0

Cyber Physical Systems, internet of things, networks

TODAY

Explosion of **data generation** + **Faster, higher-bandwidth communications** to move data around + **AI computing** to make sense of all the data and create value

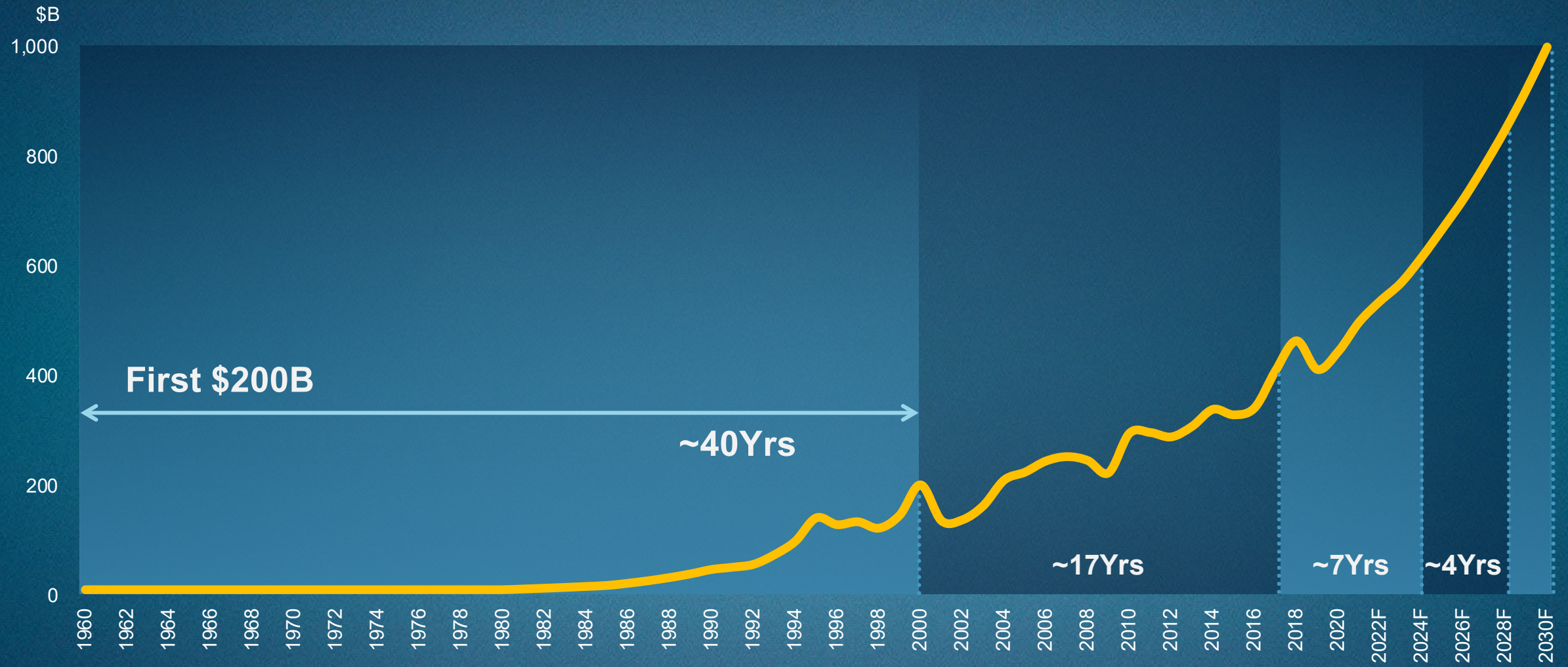
AI = ACTIONABLE INSIGHT

Semi content per unit	2015	2020	2025F
 HIGH END SMARTPHONE	$100	$170	$275
 AUTO (GLOBAL AVERAGE)	$310	$460	$690
 DATACENTER SERVER (CPU + ACCELERATOR)	$1,620	$2,810	$5,600
 SMARTHOME (GLOBAL AVERAGE)	$2	$4	$9

SILICON CONTENT GROWING AS EVERYTHING GETS SMARTER

Source: Applied Materials

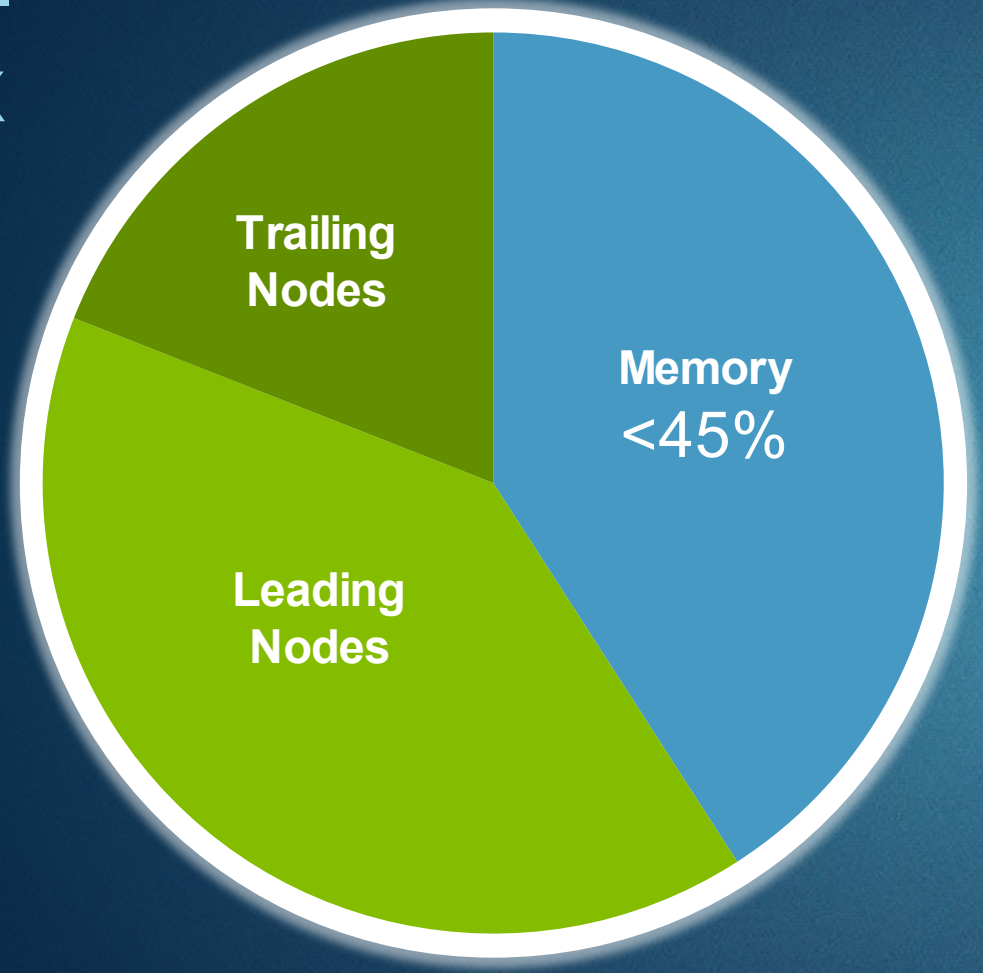
Semiconductor Industry Revenues



ACCELERATING TREND OVER TIME

Source: SEMI, VLSI, Applied Materials

Historical WFE Mix



10-Year Average

Foundry / Logic vs. Memory mix consistent over time

- 10-year and 20-year averages: Foundry / Logic >55%
- Foundry / Logic 10-year average: Leading nodes ~2/3 Trailing nodes ~1/3

Source: Gartner, VLSI, Applied Materials

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ICAPS and Packaging Technology

Sundar Ramamurthy, Ph.D.
Group Vice President
GM Epi, ICAPS and Packaging

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Applied = PPACt Enablement Company™

Unit process leadership and broadest portfolio

+

Unique combinations of technologies

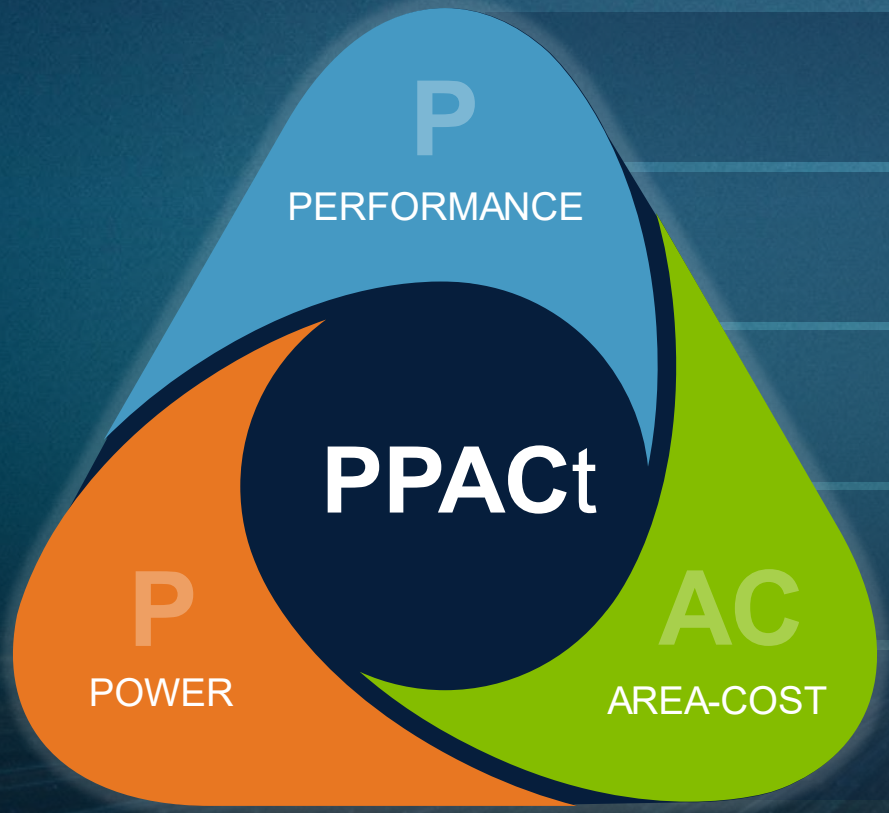
+

Actionable insight / time to market acceleration

MASTER CLASSES

ICAPS & Advanced Packaging
Today

Process Control & AppliedPRO™
Oct 18



ENABLED BY

New architectures

New structures / 3D

New materials

New ways to shrink

Advanced packaging

Time-to-Market

NEW INDUSTRY PLAYBOOK
FOUNDATION IS MATERIALS ENGINEERING

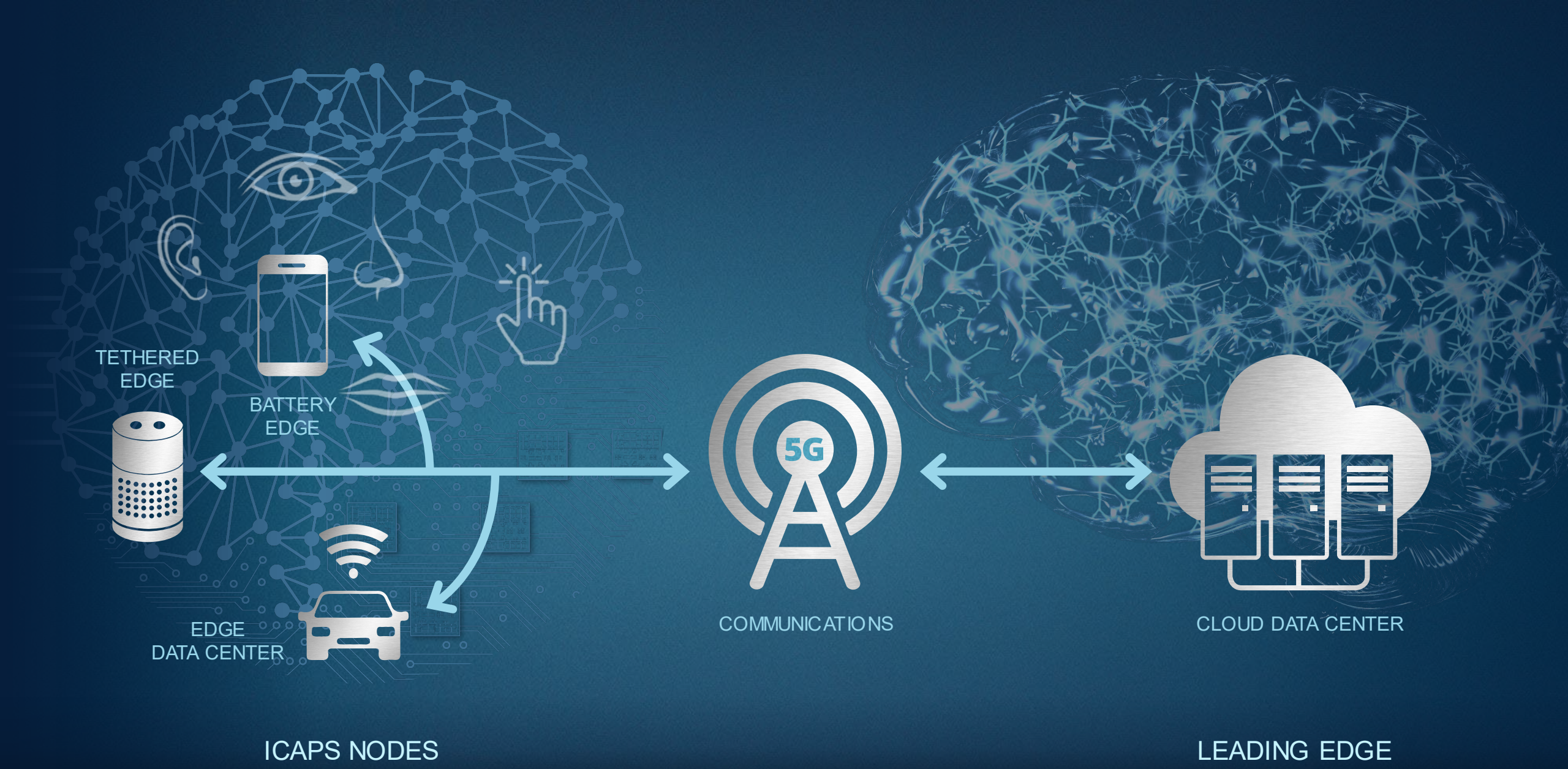
ICAPS & ADVANCED PACKAGING

ICAPS

Michael Chudzik, Ph.D.
Vice President of Technology

ADVANCED PACKAGING

Nirmalya Maity, Ph.D.
Corporate Vice President
Advanced Packaging



Unique Product Portfolio + Integrated Solutions

CREATE
Materials deposition


Epitaxy


Metal Deposition


Dielectric Deposition


Plating


ALD


Selective Deposition

SHAPE
Materials removal

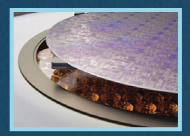

Etch


Planarization


Selective Removal

MODIFY
Materials modification


Implant


Thermal


Treatments

ANALYZE
Materials analysis

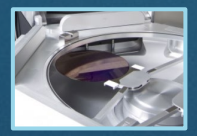

Optical Inspection


Defect Review


eBeam Inspection


CD-SEM

SOLUTIONS & CONNECTED PRODUCTS


IMS


ICAPS


Packaging


Applied AI$^{X™}$

Only company with
- Process + metrology
- Full flow chip lab
- Full flow packaging lab
- META R&D accelerator

Unique combinations
Breadth enables linking capabilities in new ways

* Applied AI$^{X™}$ is a trademark of Applied Materials

ICAPS

IoT Comms Auto Power Sensor

September 8, 2021:

“New Applied Materials Technologies Help Leading Silicon Carbide Chipmakers Accelerate the Transition to 200mm Wafers and Increase Chip Performance and Power Efficiency”

Accelerating Power Technology Roadmap

Gregg Lowe

President and CEO, Cree, Inc.

"Electrification of the transportation industry is a rising trend, and we are accelerating this inflection point by leading the global transition from silicon to silicon carbide with our Wolfspeed technology. Delivering the highest-performing silicon carbide power devices on larger 200mm wafers enables us to increase end-customer value and meet growing demand. ***Applied's support in helping speed qualification of 200mm processes in Albany and multi-equipment installations at our Mohawk Valley Fab is expediting this transition. Moreover, new technologies being developed by Applied's ICAPS team, such as hot implant, have broadened and deepened our technical collaboration and helped accelerate our power technology roadmap."***

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ICAPS Materials Engineering Challenges and Opportunities

Michael Chudzik, Ph.D.
Vice President of Technology
Semiconductor Products Group

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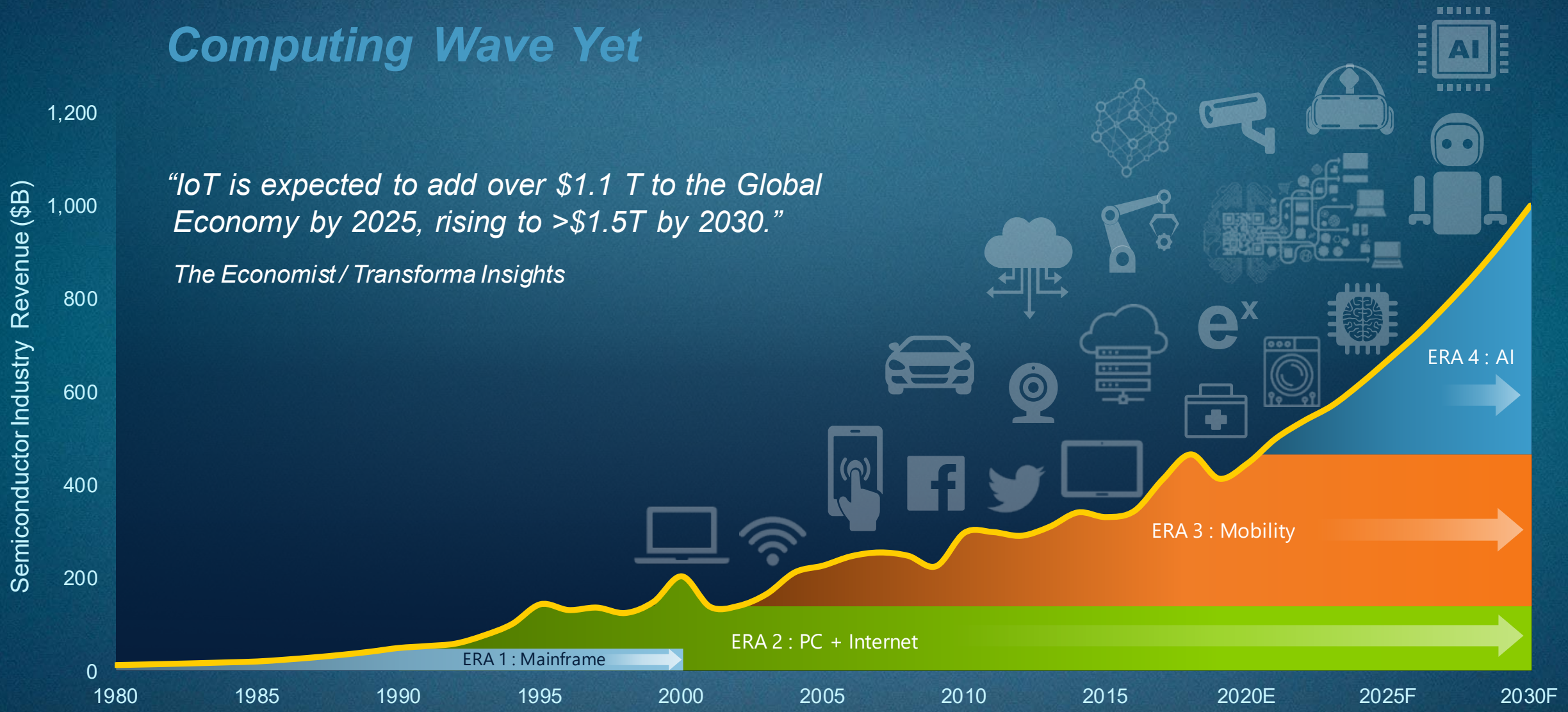
BIGGEST

Computing Wave Yet

"IoT is expected to add over $1.1 T to the Global Economy by 2025, rising to >$1.5T by 2030."

The Economist / Transforma Insights



IoT – Internet of things
PC – Personal computer
AI – Artificial intelligence

Source: SEMI, VLSI, Applied Materials

APPLIED MATERIALS

A Global Competition to Win the IoT Inflection

Global Competition

"Worldwide Spending on Edge Computing Will Reach $250 Billion in 2024"

IDC | Sep 23, 2020

"Our Wearables business is now the size of a Fortune 120 company"

Apple | Jan 27, 2021

"Microsoft earns contract worth up to $21.9 billion to make AR devices for the US Army"

CNN | Mar 31, 2021

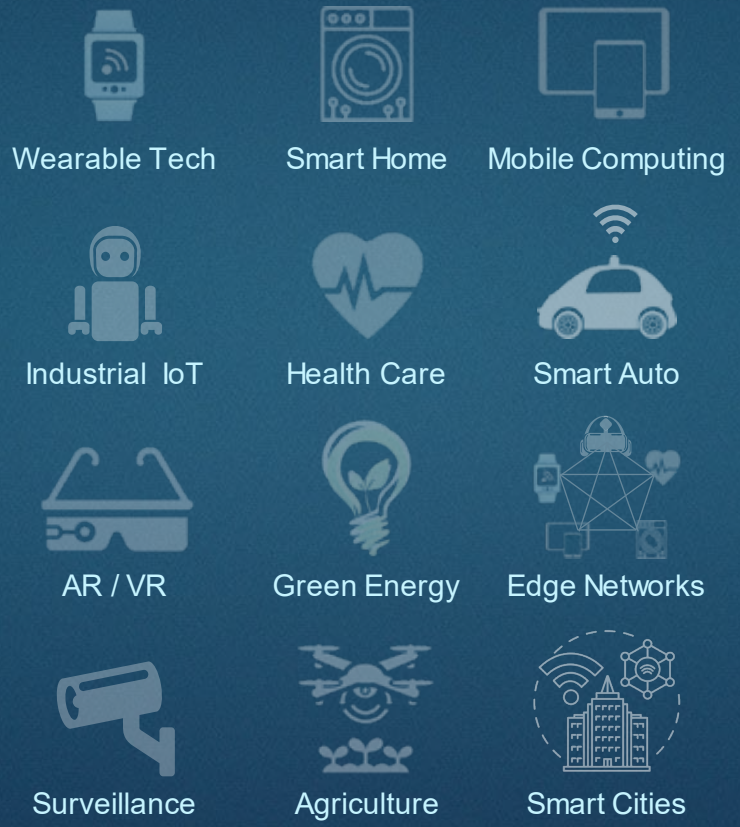
"Verizon and Honda want to use 5G and edge computing to make driving safer"

TechCrunch | Apr 8, 2021

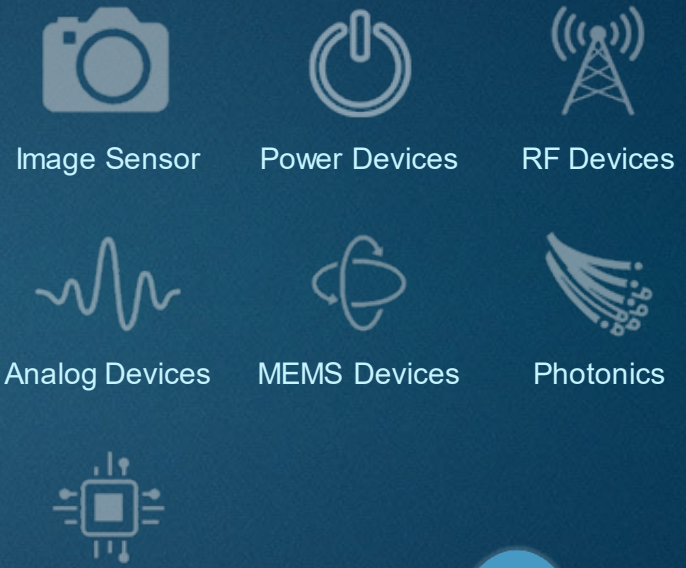
"Remote monitoring of a patient's heart and respiratory metrics is only possible with something like edge computing."

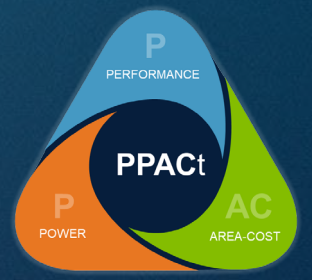
MIT | Technology Review Jun 10, 2021

New Multi-Billion-Unit Markets



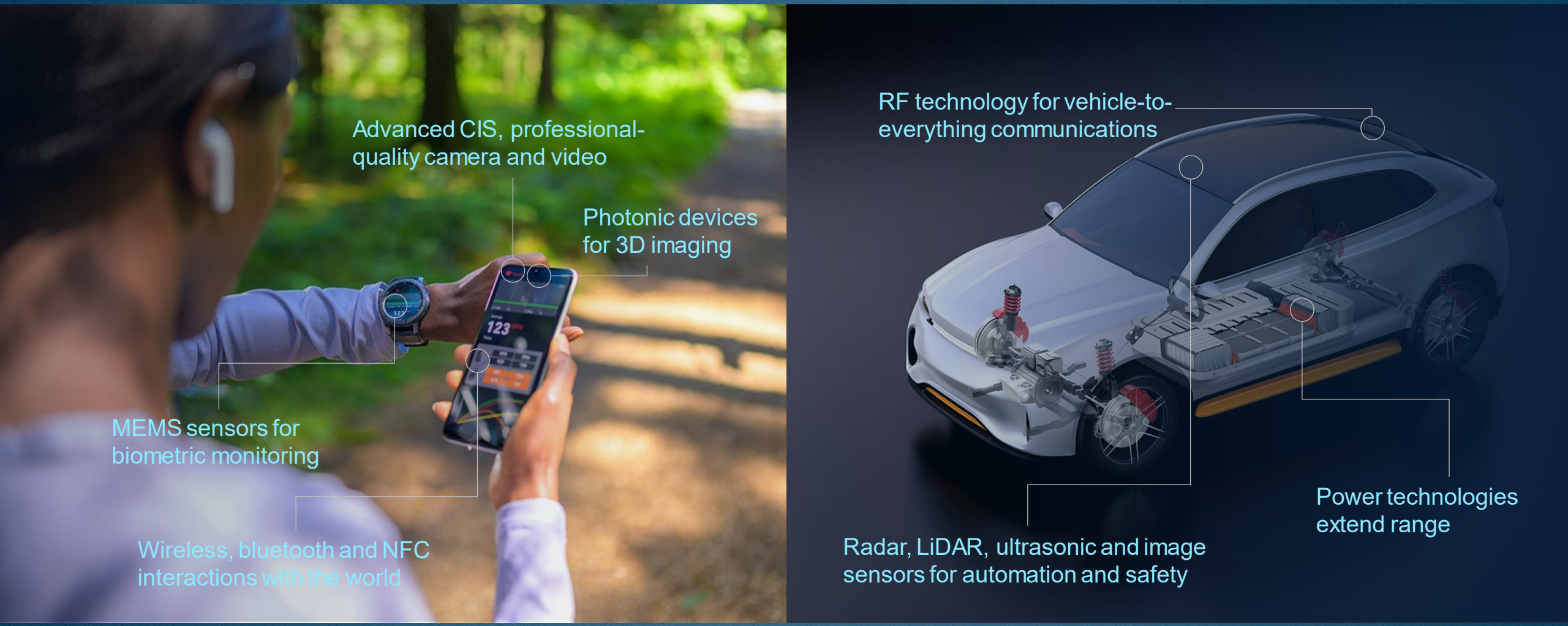
Enabled by Semi Innovations





IoT – Internet of things
AR / VR – Augmented / virtual reality
RF – Radio frequency
MEMS – Microelectromechanical systems
CMOS – Complementary metal-oxide-semiconductor

Innovative ICAPS Technologies Transforming the Edge

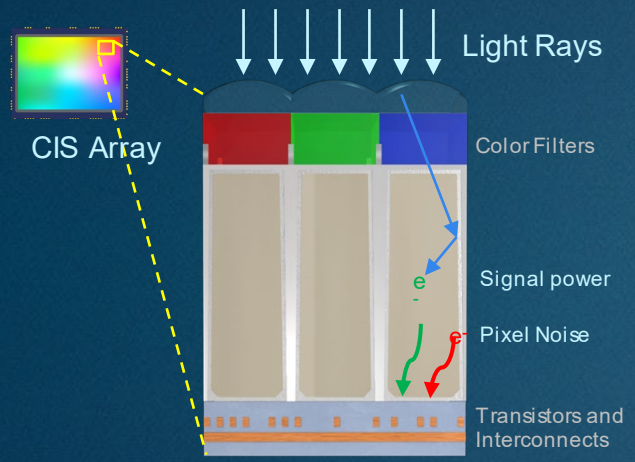


CIS – CMOS image sensor
MEMS – Microelectromechanical systems
NFC – Near-field communication
RF – Radio frequency

Image Sensor Physics and Implications for Performance

CMOS image sensor

Electrons generated in a silicon photodiode (pixel) are measured against background noise



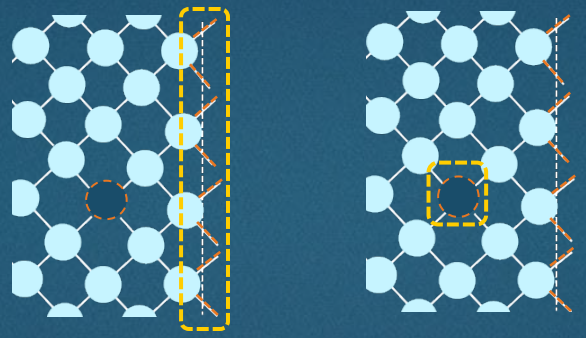
Performance is determined by the ratio of signal to noise (SNR)

$$SNR \sim \frac{Signal\ Sensitivity}{Pixel\ Noise} \propto \frac{(i_{ph}t_{int})^2}{q(i_{ph}+i_{dc})t_{int}}$$

i_{ph}: photocurrent (signal)
t_{int}: integration time
q: electron charge
i_{dc}: dark current (noise)

Pixel noise reduction

$$SNR \sim \frac{Signal\ Sensitivity}{Pixel\ Noise \sim i_{dc}}$$

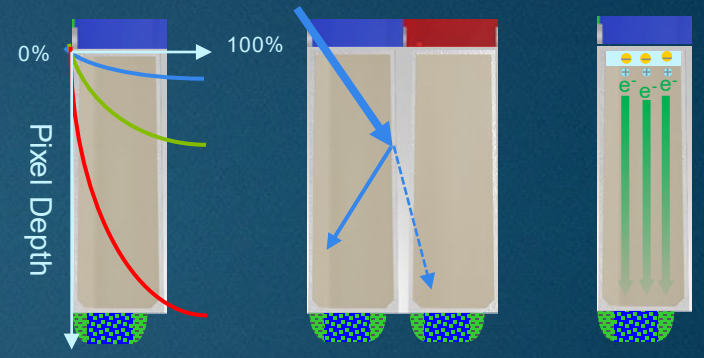


Surface damage | Crystal Damage

i_{dc} ↓
Surface damage = Interface engineering
Crystal damage = Crystal reconstruction

Signal sensitivity improvement

$$SNR \sim \frac{Signal\ Sensitivity \sim i_{ph}}{Pixel\ Noise}$$



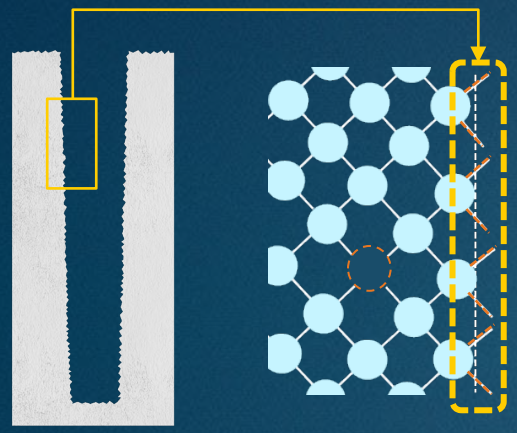
Pixel Depth | Deep Trench Isolation (DTI) | Mobility

i_{ph} ↑
Deeper Pixel = Deeper silicon trenches
New DTI materials = High reflectance
Higher mobility = Interface / bulk quality improvement

Reducing Pixel Noise with Surface Engineering

High-value problem

Defect sites at the pixel surface are sources of pixel noise



$$SNR \sim \frac{Signal\ Sensitivity}{Pixel\ Noise \sim i_{dc}}$$

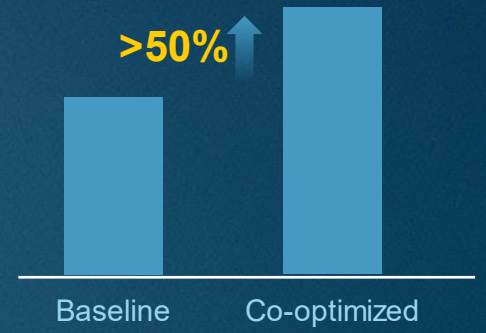
Solution

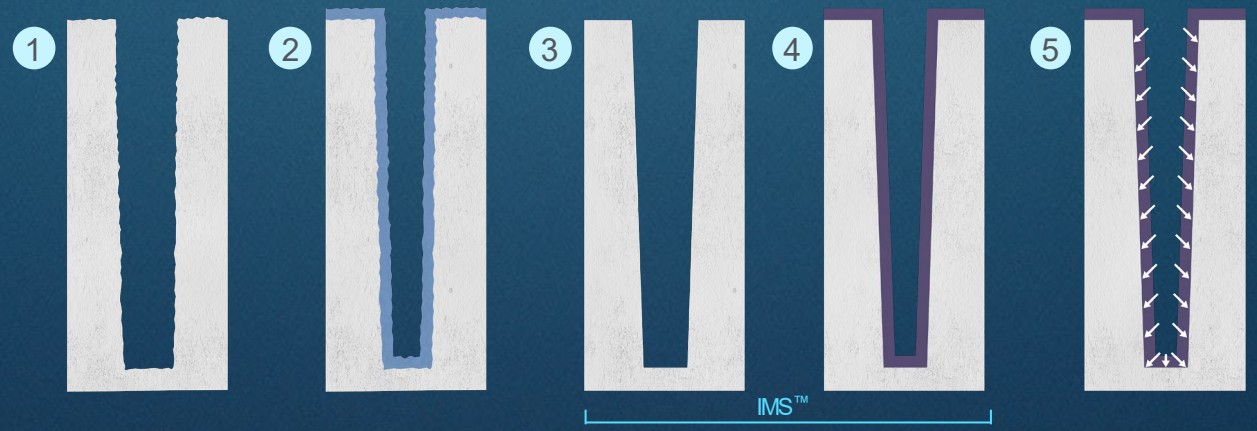
Low-damage etch followed by silicon regrowth with embedded charge sites for defect passivation

DTI surface engineering module

1. Lower damage silicon etch
2. Sidewall oxidation consumes damage layer
3. Selective removal of oxide
4. Doped epitaxial silicon regrowth
5. Millisecond anneal embeds passivating charges

Device value SNR





Products co-optimized

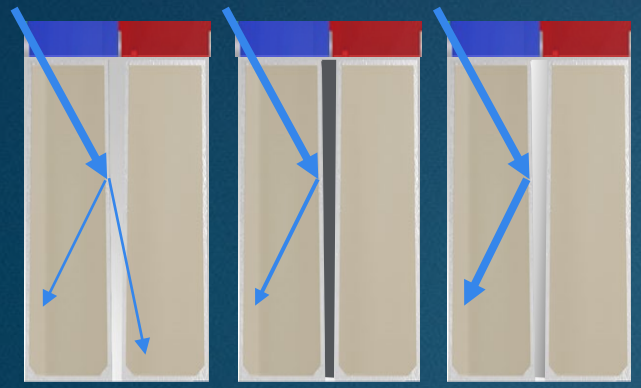
Centris® Sym3® Via Etch
Centura® RPO
Centura® RP Epi with Siconi®
Vantage® Astra® DSA

SNR – Signal-to-noise ratio
DTI – Deep trench isolation
IMS – Integrated materials solution
RPO – Remote plasma oxidation
RP – Reduced pressure
DSA – Dynamic surface anneal

Improved Signal Sensitivity with New Materials for DTI

High-value problem

Signal sensitivity is degraded when incoming light escapes the pixel or is absorbed by the blocking layer



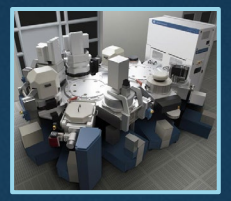
	Technology	Light Blocking	Light Reflecting
Gen 1	Dielectric Refraction	● ○ ○	● ○ ○
Gen 2	Tungsten Metal Blocking	● ● ●	● ○ ○
Gen 3	Aluminum Metal Reflectance	● ● ●	● ● ●

Solution

DTI created with a highly reflective aluminum layer co-optimized with pre- and post- processes to maximize signal current

DTI aluminum reflectance module

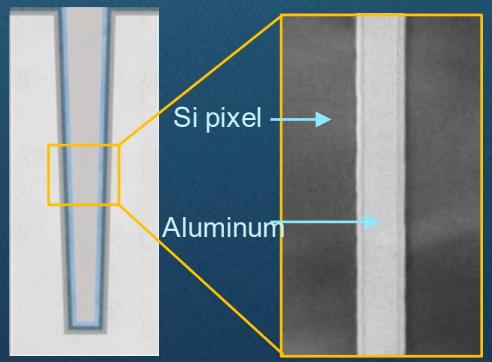
1 ALD Liner + CVD Al deposition



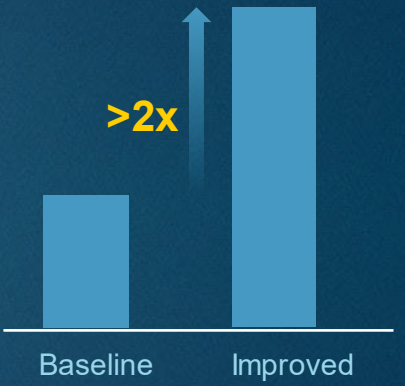
IMS™

2 Aluminum Planarization

ALD Liner + CVD Al inside DTI



Quantum efficiency



Products co-optimized

Endura® CVD Al

Reflexion® LK CMP

DTI – Deep trench isolation IMS – Integrated materials solution
ALD – Atomic layer deposition CVD – Chemical vapor deposition

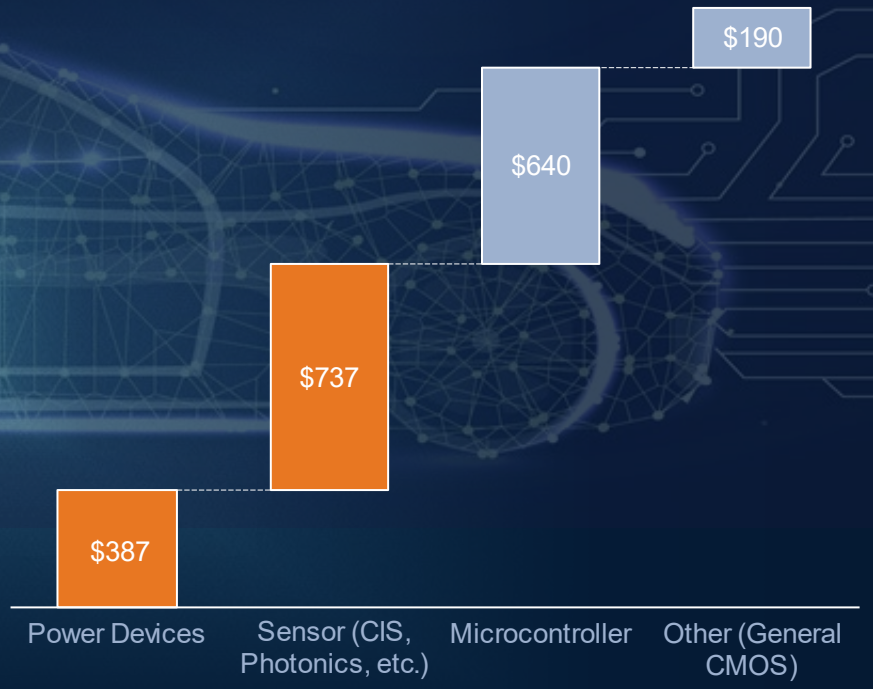
Transition to EV with adoption of ADAS increases ICAPS semiconductor content by 4x

Internal Combustion Engine[1]

~$500 Total cost

47% Power & Sensors

Electric Vehicle[2]



~$2,000 Total cost

58% Power & Sensors

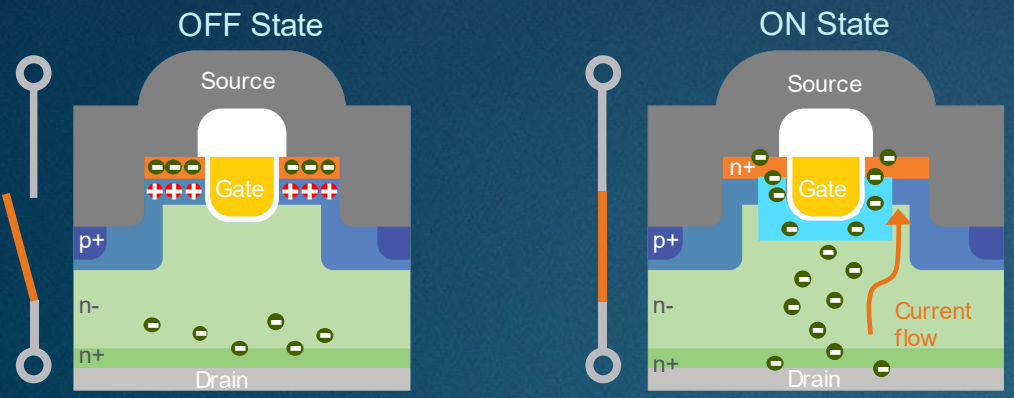
EV – Electric vehicle
ADAS – Advanced driver-assistance systems
CIS – CMOS image sensor
CMOS – Complementary metal-oxide-semiconductor

1 Based on ADAS L2 Content
2 Based on ADAS L4/5 Content
Source: Infineon ATD report, 2015, 2020

Power Device Physics and Implications for Performance

Power MOSFET

A high-voltage, high-current semiconductor switch



Most critical challenge is to reduce power losses in the switch

$$\text{Power Dissipation} = I_D{}^2 \cdot R_{ON}$$

$$R_{ON} = \frac{w_D}{q\mu_n N_D}$$

I_D : Drain current
R_{ON} : On resistance
w_D : Depletion region width
q : Proton charge
μ_n : Electron mobility
N_D : Dopant concentration

MOSFET – Metal-oxide-semiconductor field-effect transistor

Improving power MOSFET performance

$\downarrow R_{ON}$

Increase mobility μ_n

Material selection (Si, SiC, GaN), crystal orientation

Minimize crystal defects in the bulk or at the surface

Increase dopant concentration N_D

Implant dose / minimizing implant crystal damage

Tradeoff between performance and cost

	Si	SiC	GaN
Breakdown Voltage	1x	10x	25x
Device Efficiency	●○○	●●○	●●●
Relative Die Size	10x	1x	≤ 1x
Wafer Cost (size)	$30 (6”)	$800 (6”)	$1200 (4”)
% Contribution to Market Growth (‘20-’26)	36%	48%	16%

Applied Materials estimates, Yole Developpement and Omdia

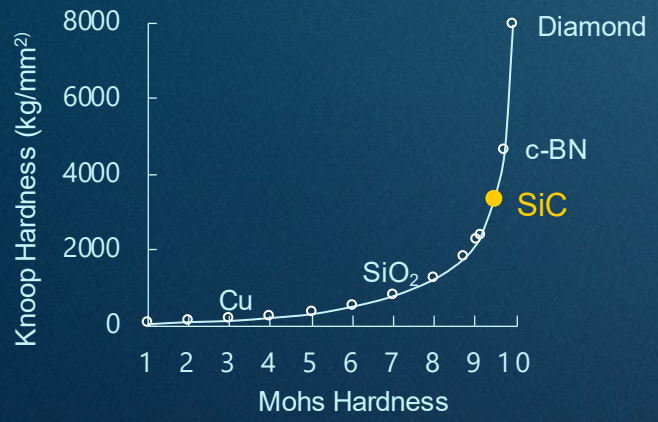
Reducing Surface Defects | Why This is Difficult

High-Value Problem

Electron mobility is degraded by crystal defects originating from the SiC substrate

O. Kordina, Silicon Carbide Epitaxy, 2012

Hardness of SiC makes polishing extremely challenging

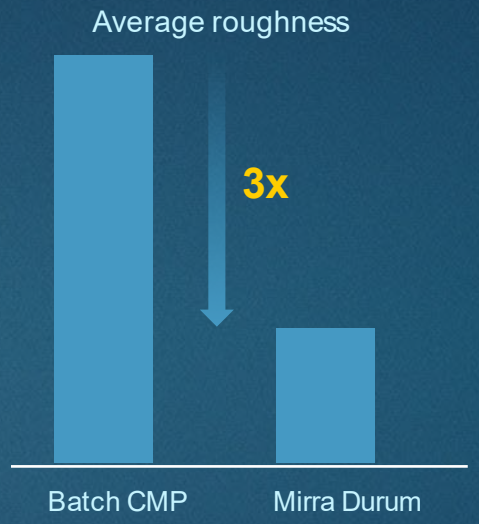


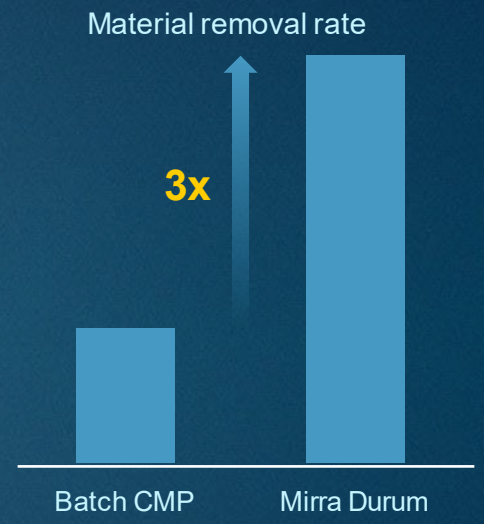
Solution

Single-wafer CMP with higher down force and optimized consumables to minimize surface defects

Pre-CMP
High density of scratches

Post-CMP
Scratch-free





Mirra® Durum™ CMP

- Highest productivity single-wafer multi-platen polisher for SiC
- Processes both 150mm and 200mm wafers
- Fully automated dry-in, dry-out wafer handling
- Integrated cleaning, drying and metrology

CMP – Chemical mechanical planarization

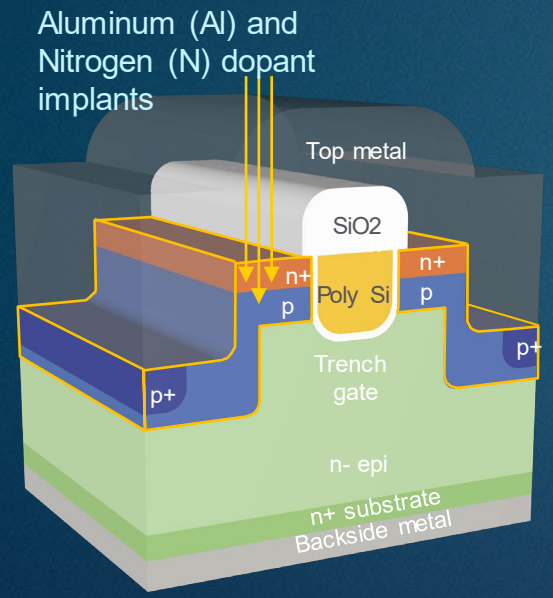
Increasing SiC MOSFET Mobility and Lowering Resistance

High-Value Problem

Bulk defects in SiC caused by implant damage reduce electron mobility

$$R_{ON} = \frac{w_D}{q\mu_n N_D}$$

I_D : Drain current
R_{ON} : On resistance
w_D : Depletion region width
q : Proton charge
μ_n : Electron mobility
N_D : Dopant concentration

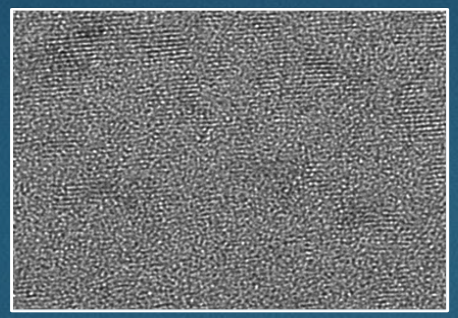


Conventional implanting of dopants damages the crystal lattice

Solution

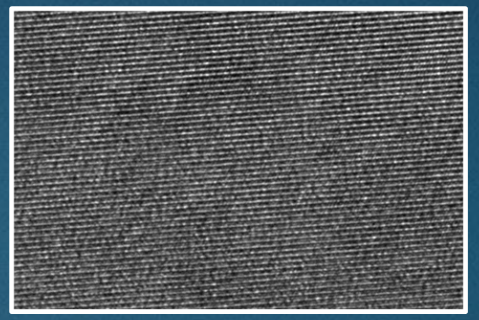
Room-temperature implant damages crystal; hot implant allows crystal damage to *heal*, reducing R_{ON}

Amorphized structure
Damaged



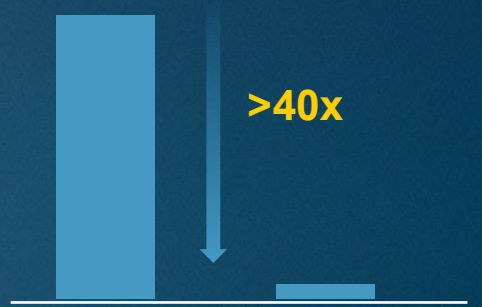
25 ˚C implant

Crystallized structure
Healed



500 ˚C implant

Resistivity*



VIISta® 900 3D

- Highest productivity implanter for 150mm and 200mm SiC
- Hot implant capability for bulk damage reduction
- Tilted implant for next-generation SiC device architectures
- Solid dopant Al ion source for lowest maintenance time

* Post 1600°C Anneal

MOSFET – Metal-oxide-semiconductor field-effect transistor

Organized to Address ICAPS Opportunities

Unit process leadership and broadest portfolio


Metal Deposition


Epi


Implant


Etch


Planarization

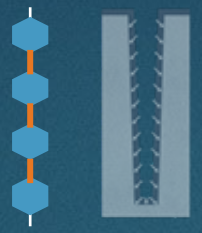

Inspection

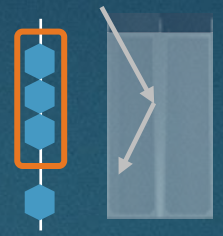

Dielectric Deposition


Various Wafer Sizes

+

Unique combinations of technologies


Co-optimization of processes / tools


Integrated materials solutions

+

Time-to-market acceleration


Dedicated and partner ICAPS device labs/fabs


Device Modeling


Test Structures

Dedicated technical collaboration with our customers to accelerate their PPACt roadmaps

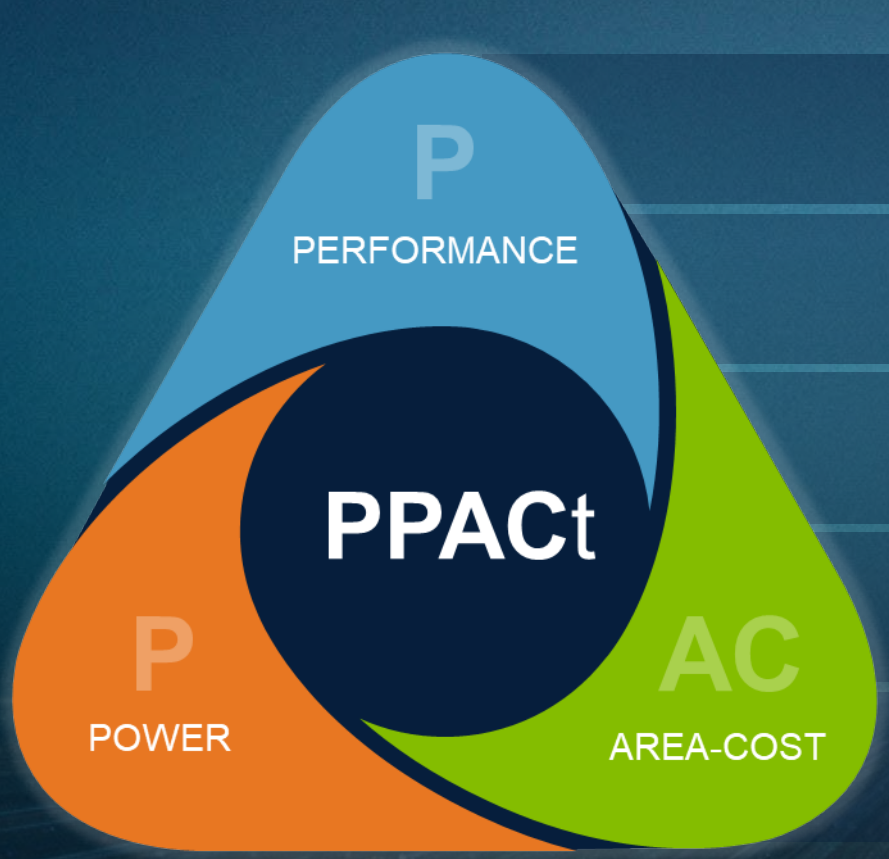
APPLIED MATERIALS®
make possible

Advanced Packaging Challenges and Opportunities

Nirmalya Maity, Ph.D.
Corporate Vice President Advanced Packaging

ICAPS and PACKAGING MASTER CLASS | September 8, 2021

APPLIED MATERIALS®



ENABLED BY

New architectures

New structures / 3D

New materials

New ways to shrink

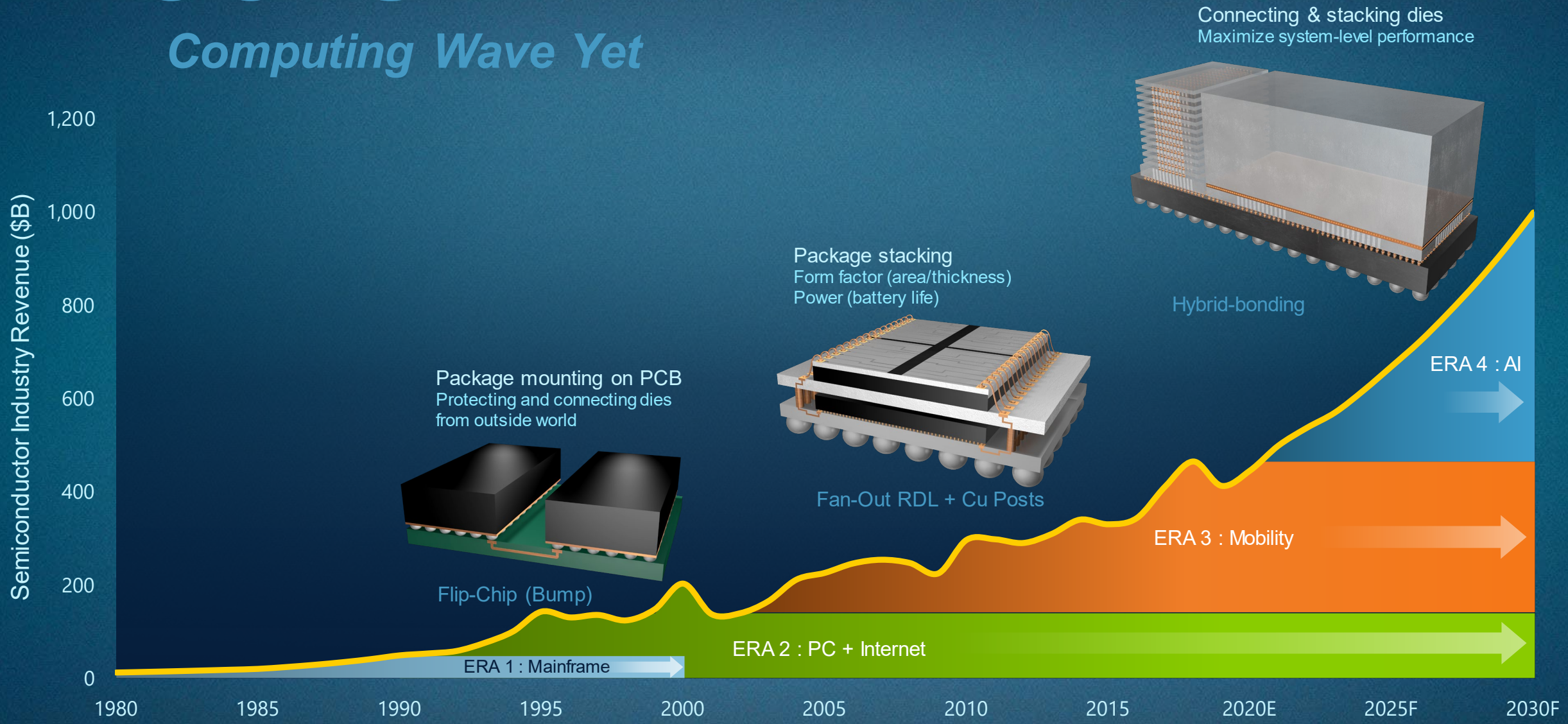
Advanced packaging

Time-to-Market

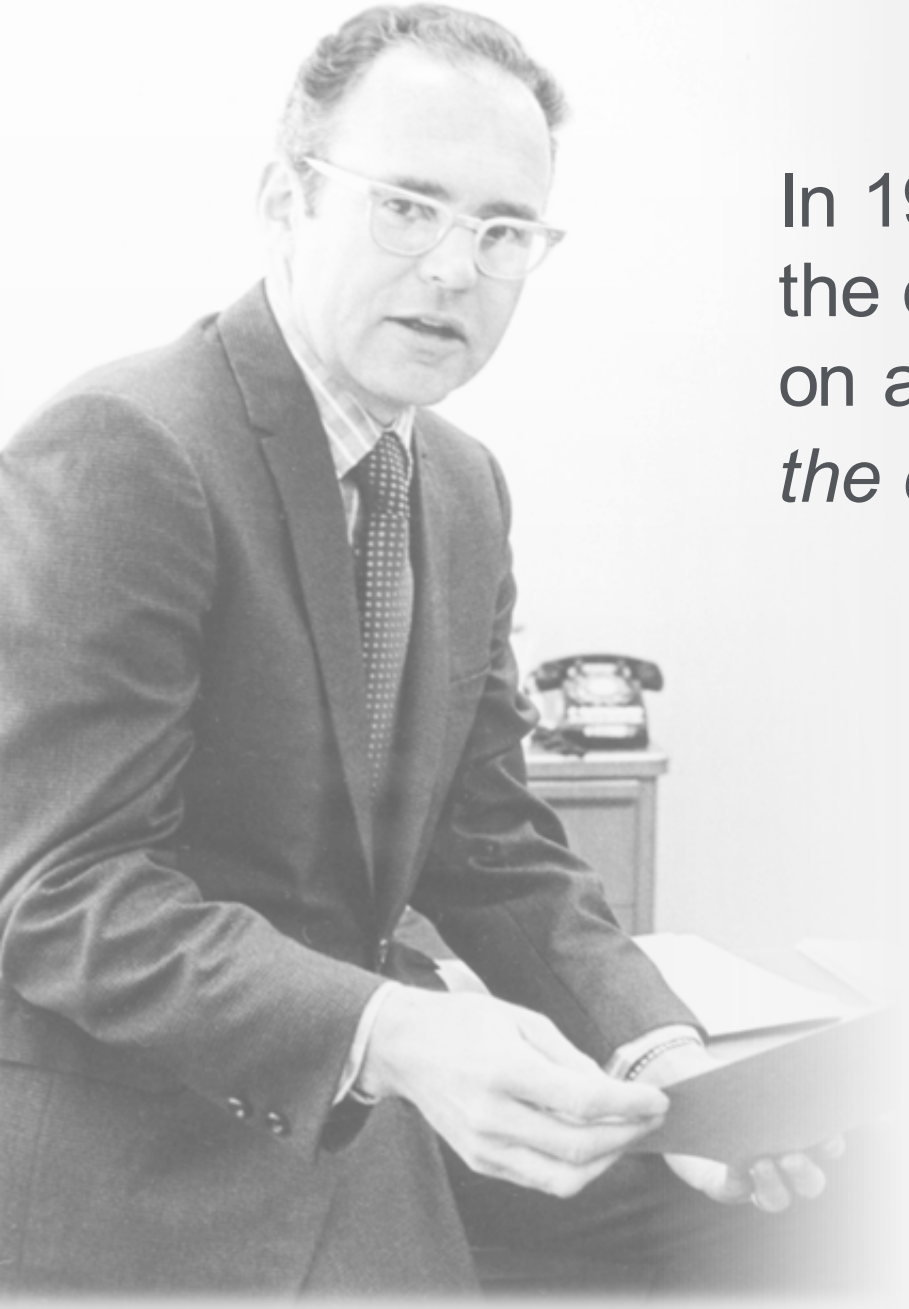
NEW INDUSTRY PLAYBOOK
FOUNDATION IS MATERIALS ENGINEERING

BIGGEST

Computing Wave Yet



Source: SEMI, VLSI, Applied Materials



In 1965, Gordon Moore predicted both the exponential increase of transistors on a chip, and conditions that would drive *the disaggregation of the system-on-chip*

> “It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”

https://archive.computerhistory.org/resources/access/text/2017/03/102770822-05-01-acc.pdf

Packaging Enables PPACt™ Scaling

Power
Performance
Area

Shorter, parallel interconnects

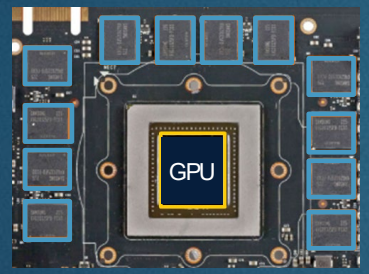
Higher I/O
Reduced latency
Lower power

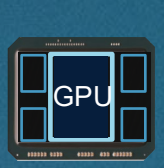
30x lower power

PCB chip-to-chip connection vs. hybrid bonding

3D stacking

Tighter integration
Many chips per package
High bandwidth





~3X system performance
>50% lower power

Compared to disaggregated dies on a PCBs

Source: Samsung whitepaper

Cost
time-to-market

Chiplets

Higher yield
Reuse IP blocks

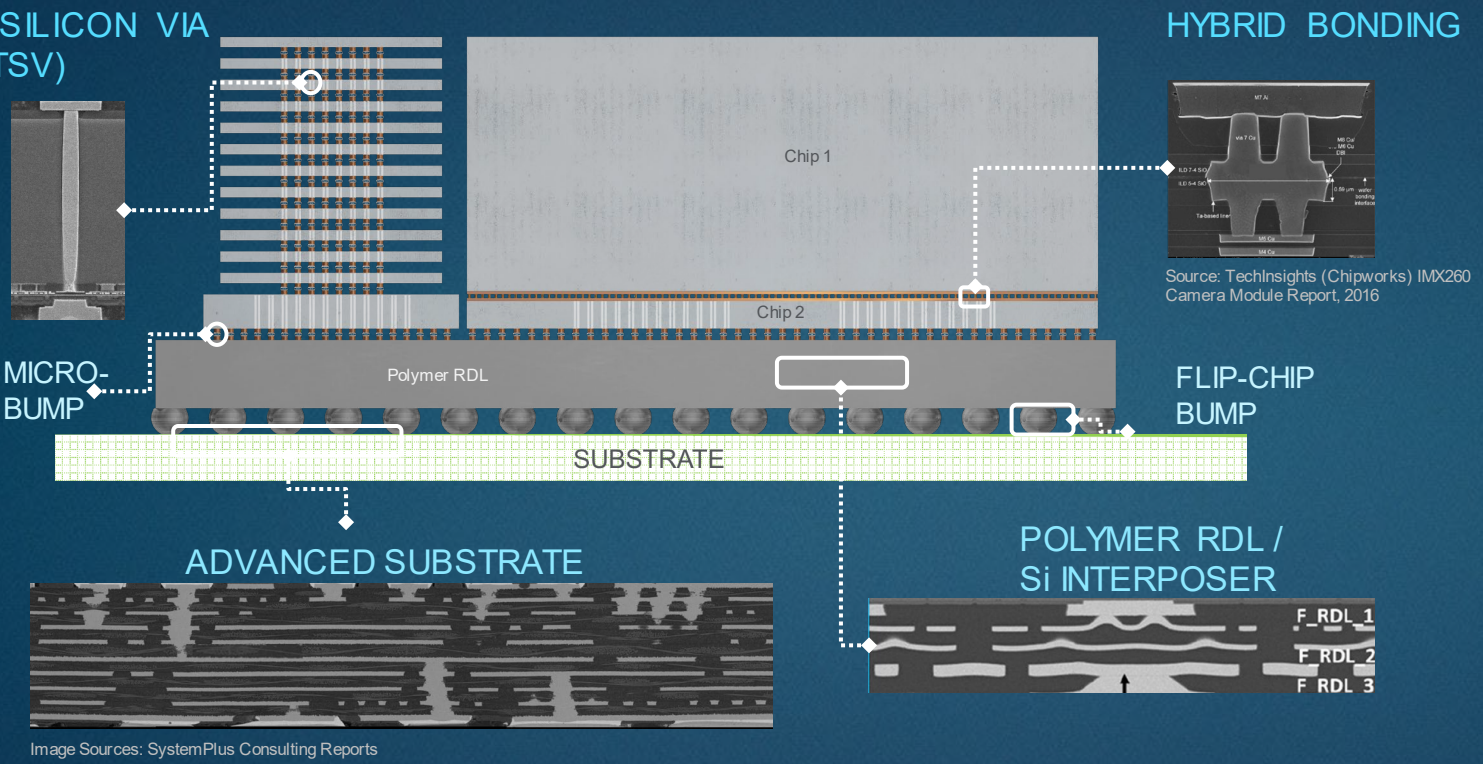
~60% lower cost

vs. 900mm die partitioned into 3 and 3D stacked

Compared to large and specialized SOC chips

Source: A. Steengen, IMEC (Semicon Korea 2018)

System Integration with Emerging 2D and 3D Interconnects



Source: TechInsights (Chipworks) IMX260 Camera Module Report, 2016

Image Sources: SystemPlus Consulting Reports

3D Interconnects

- Through-Silicon Via (TSV)
- Hybrid bonding[1]

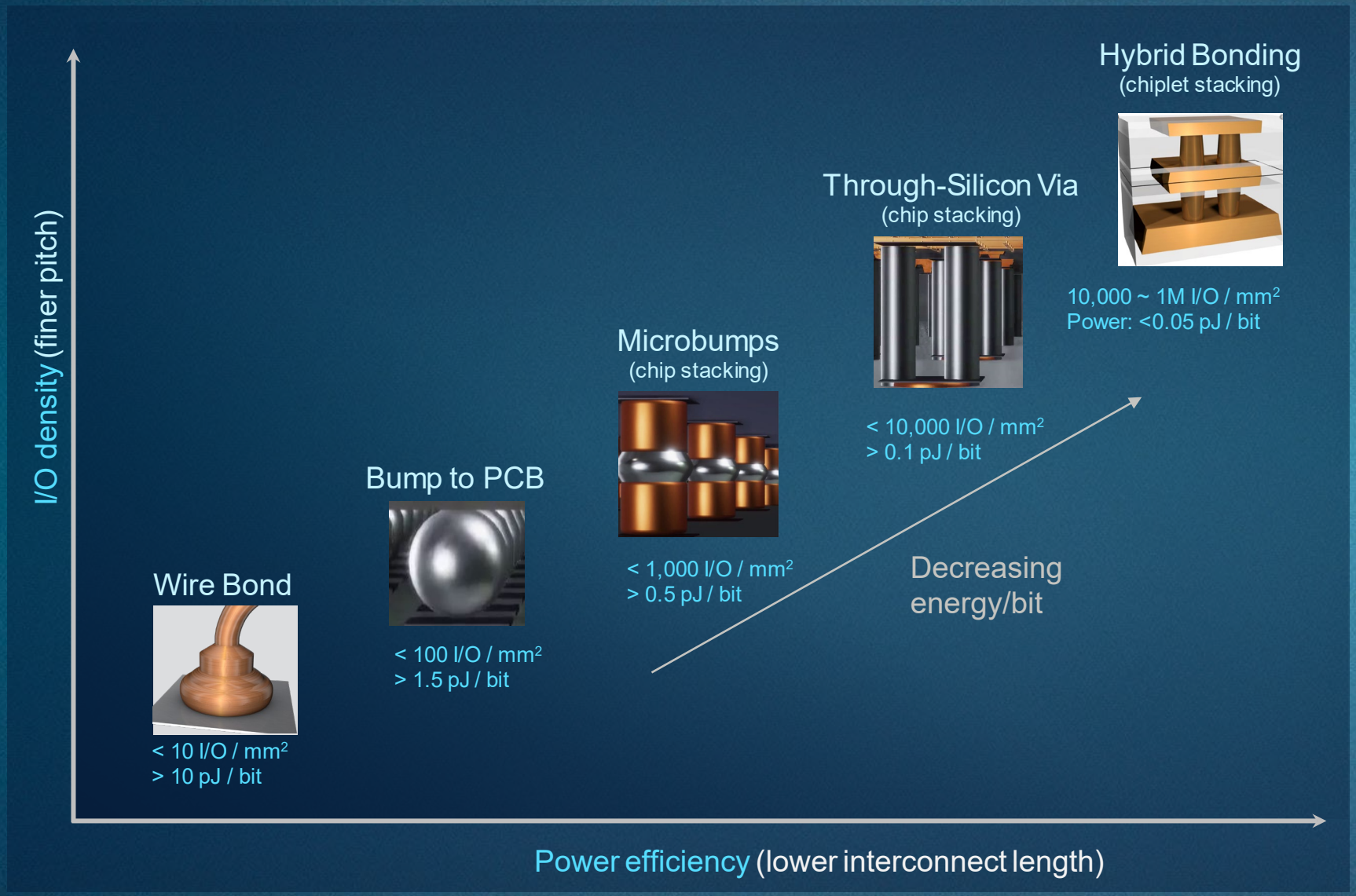
2D Interconnects

- Redistribution layer (RDL) on wafer or panel[1]
- Advanced substrate[1]

1 Emerging inflection

Multiple inflections + higher process complexity, needs broad technology portfolio and integrated solutions

Packaging System Interconnect Scaling Roadmap



Better power efficiency w/ finer pitch, shorter lengths

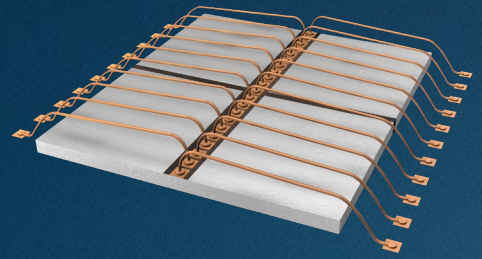
Hybrid bonding reduces lengths to micron scale

Future integration:
Logic + Memory + PMIC

Packaging to Enable Higher Density and Performance

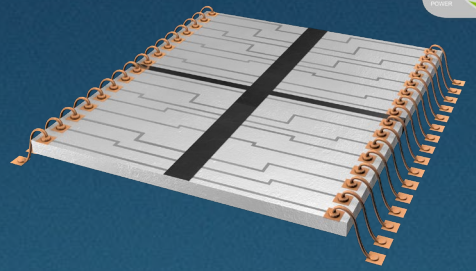
Top View

Connections initiate from DRAM die center



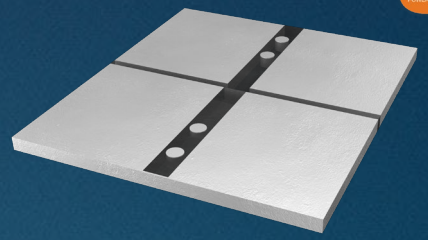
Single or two die wire-bonded onto package

Redistribution layer routes connections to edge



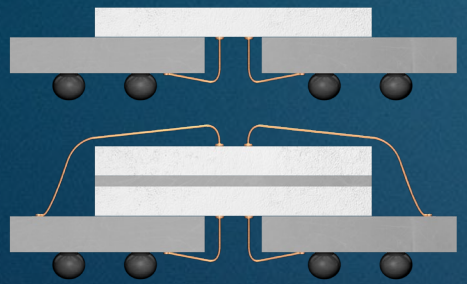
2-4 die on package
Aluminum RDL and wire-bonded

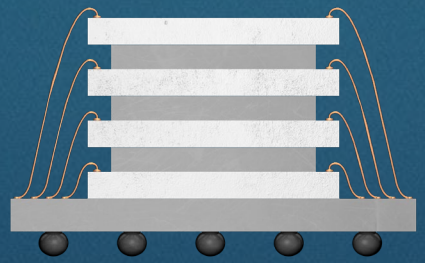
TSV routes connections through silicon die



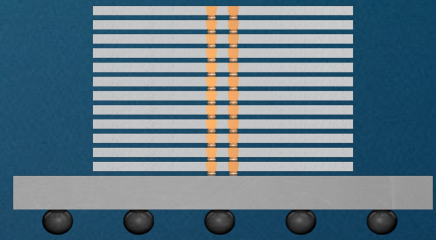
4+ die on package
Connected by TSVs and micro-bumps

Side View





Enabling technologies
Endura® PVD



Enabling technologies
TSV and micro-bump processes

3X growth in DRAM wafers using advanced schemes like flip-chip, stacking or TSV stacking by 2025

Source: Applied Materials estimates

Through-Silicon Via Fabrication and Backside Reveal

TSV Formation

Centris® Sym3® Via Etch

Producer® InVia® CVD

Endura® Ventura® PVD

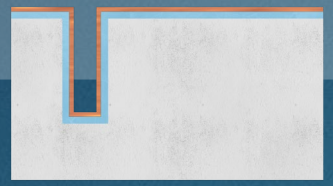
Nokota® Raider® ECD

Reflection® LK CMP

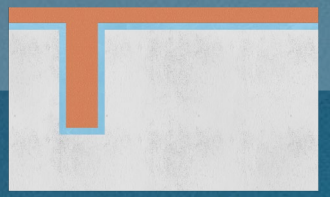
Incoming Wafer

TSV Etch Bottom Open (Via Last)

CVD Liner



PVD Barrier and Seed



TSV Cu Plating

Planarize Remove Cu/Barrier

Backside Reveal

Reflection® LK CMP

Centris® Sym3® Via Etch

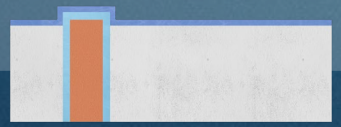
Producer® InVia® CVD

Reflection® LK CMP

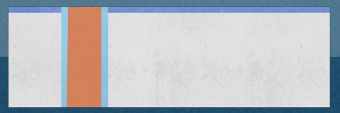
Thinned Wafer

Silicon Polish

Recess Etch



CVD Passivation

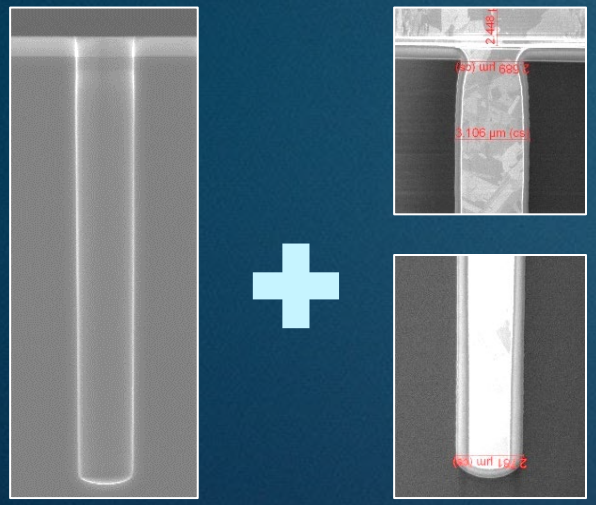


Copper & Oxide Polish

Redistribution Layer & Bump/Fan-Out

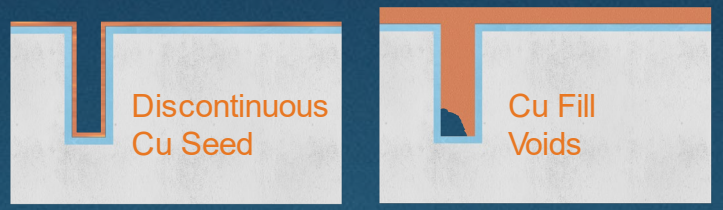
Solving TSV Extendibility Challenges

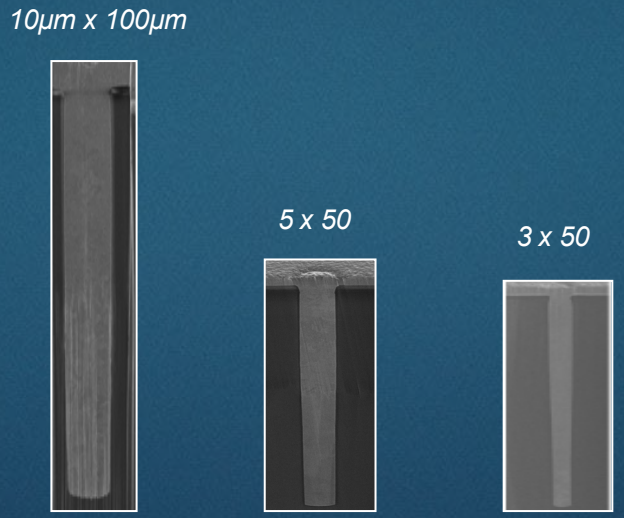
Electrical Isolation at Low Temperatures



Smooth silicon sidewall and high-quality dielectric liner

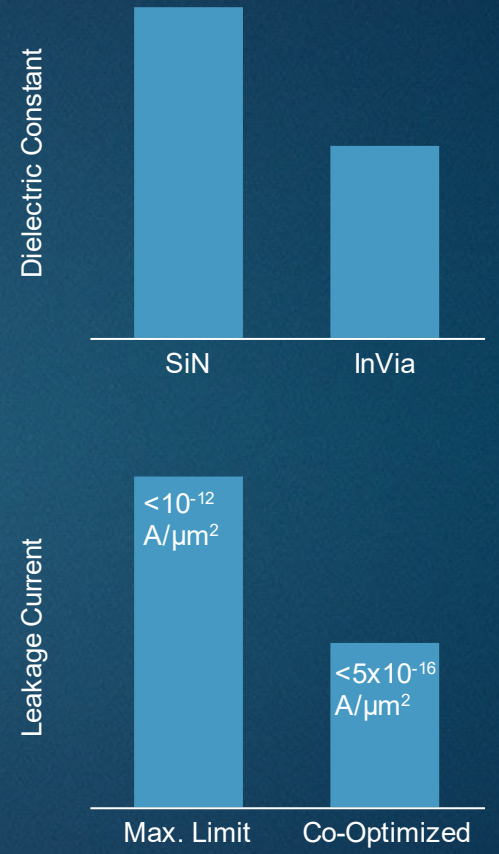
Complete TSV Fill with Copper





Co-optimization of PVD liner and ECD fill for robust TSV gap-fill extendable to 3x50 vias

Co-Optimizing Processes

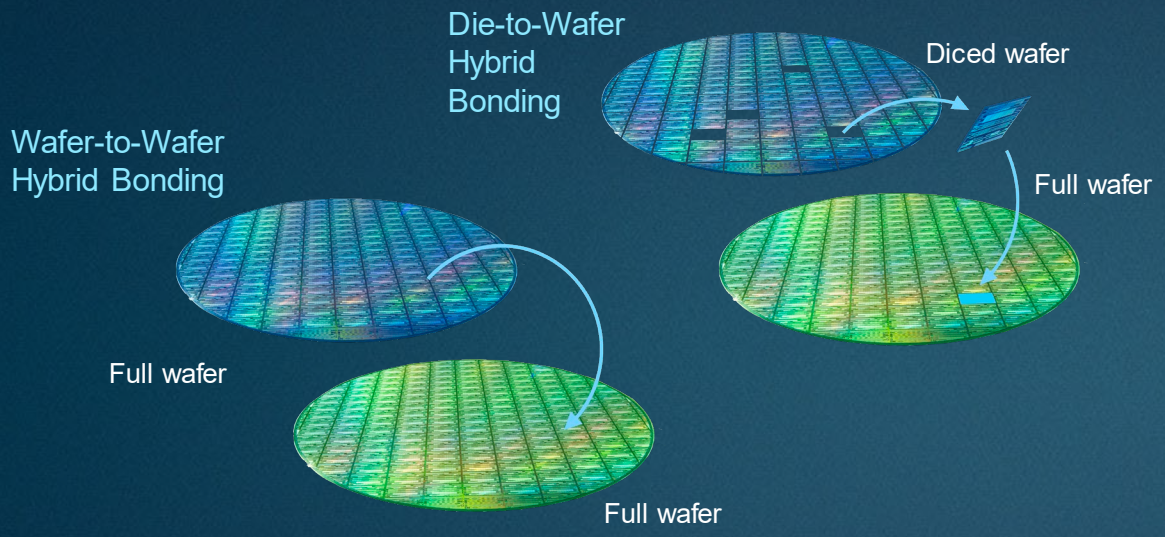


Electrically robust solution

Hybrid Bonding: Enabling 10K-1M/mm^2 I/O Density Paradigm

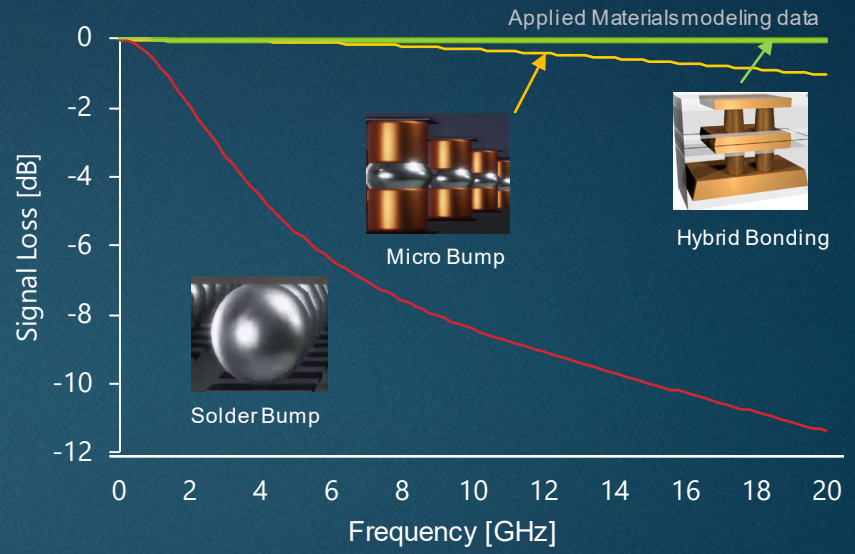
What is hybrid bonding?

Shortest connections with face-to-face chip bonding



The potential of hybrid bonding

Ultimate bonding solution – outstanding performance



The challenge

Making over 10,000 connections simultaneously with defect-free copper bonding
Die-to-wafer and wafer-to-wafer alignment – at an economical cost

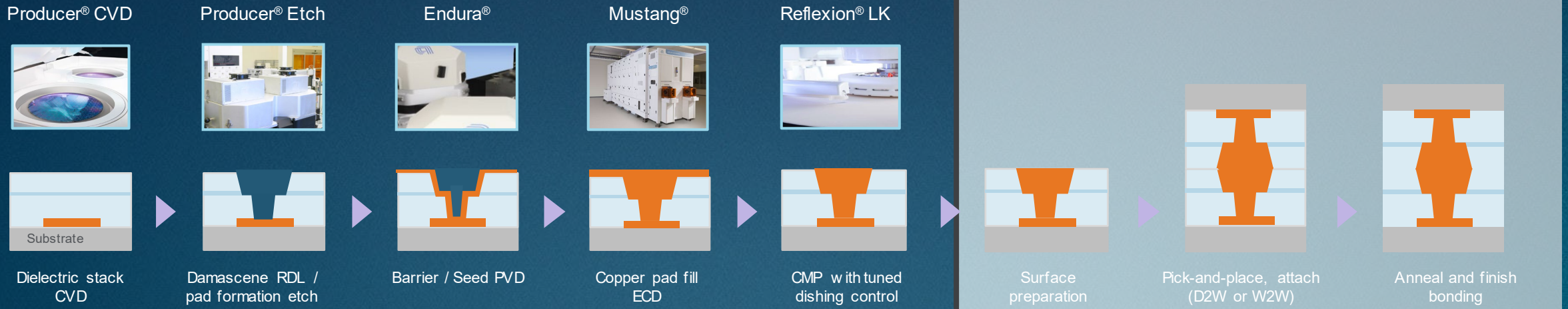
Enabling hybrid bonding in collaboration with Besi die-to-wafer and EVG for wafer-to-wafer

Optimization of Complete Process for Highest Bonding Yield

Pad Formation: current Applied Materials product portfolio

+

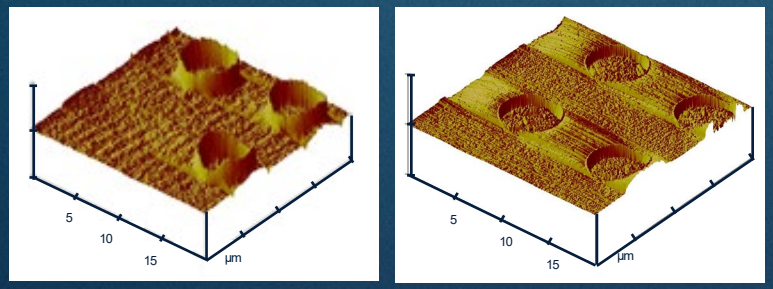
Bonding: in partnership



Engineered surface profile

① Material polish rate differences

② Optimized copper pad recess

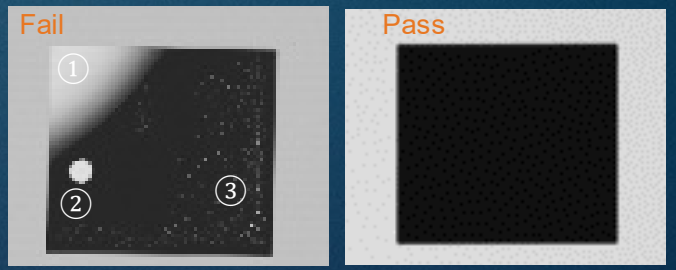


Surface preparation and bonding

① Edge delamination

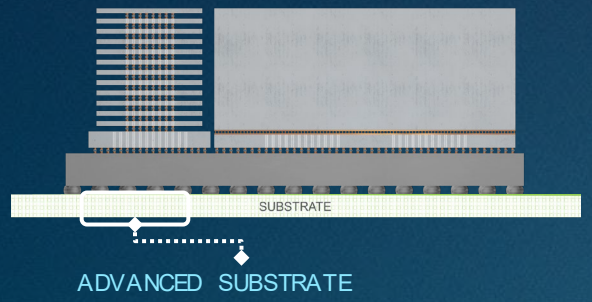
② Large void

③ µ-void

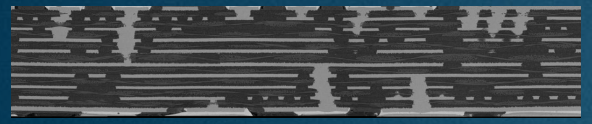


Processing Large Packages and Substrates

System integration of multiple chips on package



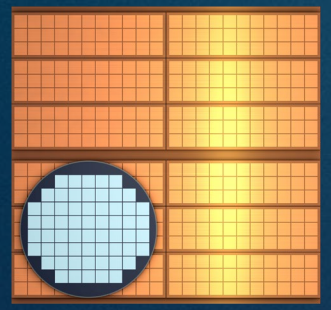
Panel-level packaging
Package size grows

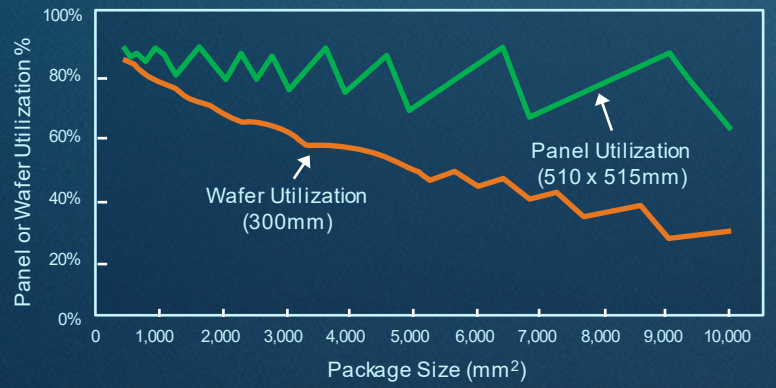


Semi quality processing
Higher I/O density requires interconnects to shrink

Image Sources: SystemPlus Consulting Reports

Better substrate utilization as package sizes increase





Source: Intel

Advanced large substrate PVD technology

Applied Topaz™ PVD

Acquisition of Tango Systems Panel PVD technology

Panels up to 600x600mm
Thin panel handling capability

Leveraging decades of Applied PVD technology leadership in both semiconductor and large format display businesses

Enabling fine-line interconnects in large-format packaging substrates

Organized to Address Packaging Challenges

Unit process leadership and broadest portfolio

+

Focus on enabling valuable inflections

+

Co-optimized technologies


Metal Deposition

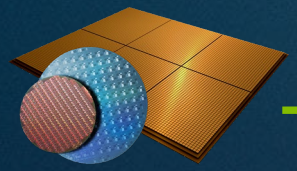

Dielectric Deposition


Plating


Etch

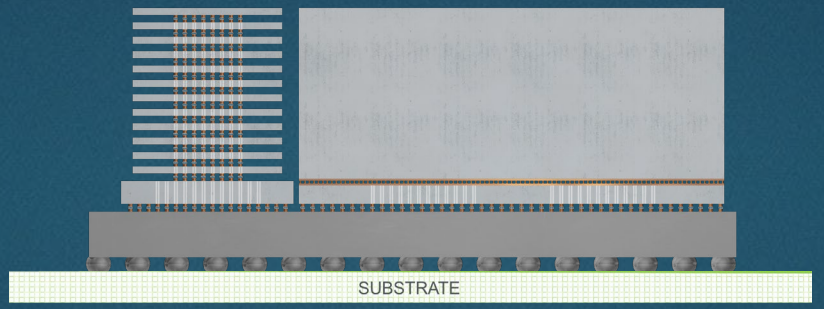

Planarization


Inspection


Wafer and Panel

+


Partnerships

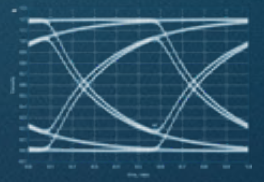


Heterogeneous Integration

Advanced Substrates

Uniquely positioned to capture growth from inflections


Dedicated advanced packaging lab


Package modeling


Test vehicles

APPLIED MATERIALS®
make possible

ICAPS and Packaging Growth Opportunities

Sundar Ramamurthy, Ph.D.
Group Vice President
GM Epi, ICAPS and Packaging

ICAPS and PACKAGING MASTER CLASS | September 8, 2021

APPLIED MATERIALS®

Going Beyond Unit Process Tools to Deliver Solutions

FASTER TIME TO MARKET, HIGHER VALUE, STICKIER

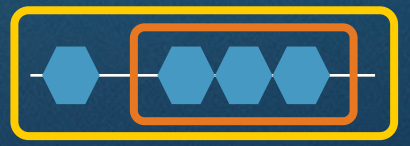
UNIT PROCESS LEADERSHIP
+ BROADEST PORTFOLIO

CO-OPTIMIZATION OF
PROCESSES / TOOLS

~40% of our products
now co-optimized

INTEGRATED
MATERIALS
SOLUTIONS

~30% of our products
now integrated

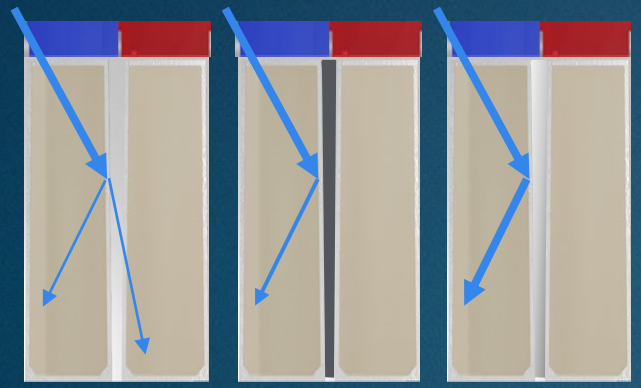


ACTIONABLE INSIGHT
ACCELERATION

Improved Signal Sensitivity with New Materials for DTI

High-value problem

Signal sensitivity is degraded when incoming light escapes the pixel or is absorbed by the blocking layer



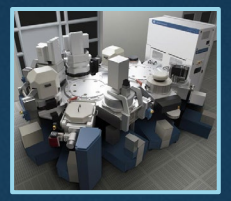
	Technology	Light Blocking	Light Reflecting
Gen 1	Dielectric Refraction	● ○ ○	● ○ ○
Gen 2	Tungsten Metal Blocking	● ● ●	● ○ ○
Gen 3	Aluminum Metal Reflectance	● ● ●	● ● ●

Solution

DTI created with a highly reflective aluminum layer co-optimized with pre- and post- processes to maximize signal current

DTI aluminum reflectance module

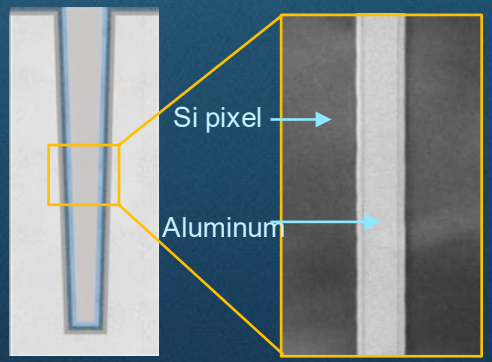
1 ALD Liner + CVD Al deposition



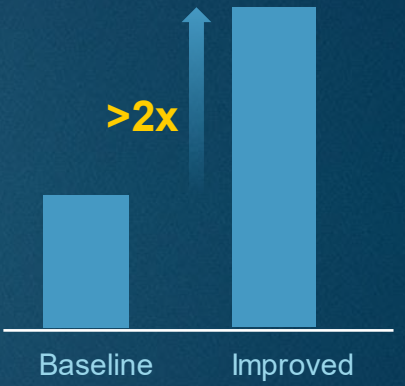
IMS™

2 Aluminum Planarization

ALD Liner + CVD Al inside DTI



Quantum efficiency



Products co-optimized

Endura® CVD Al

Reflexion® LK CMP

DTI – Deep trench isolation IMS – Integrated materials solution
ALD – Atomic layer deposition CVD – Chemical vapor deposition

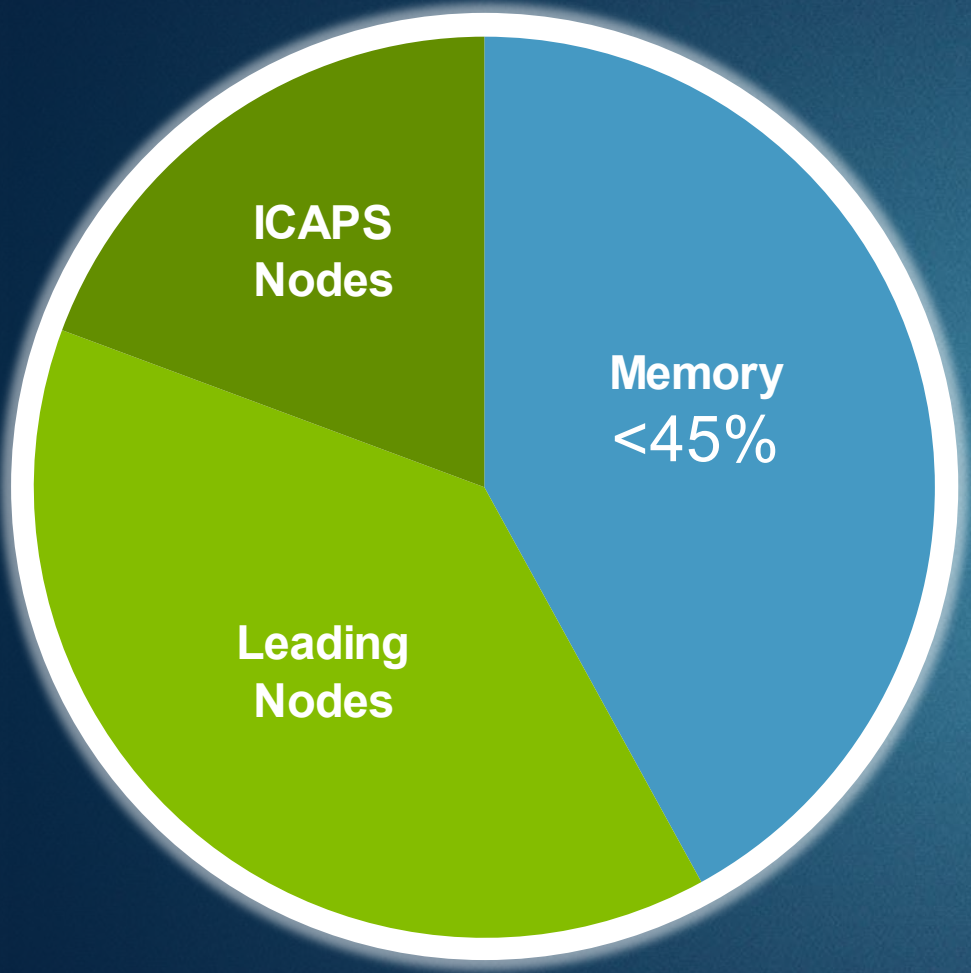
New Materials Co-Optimized to Improve CIS Capabilities

Terushi Shimizu

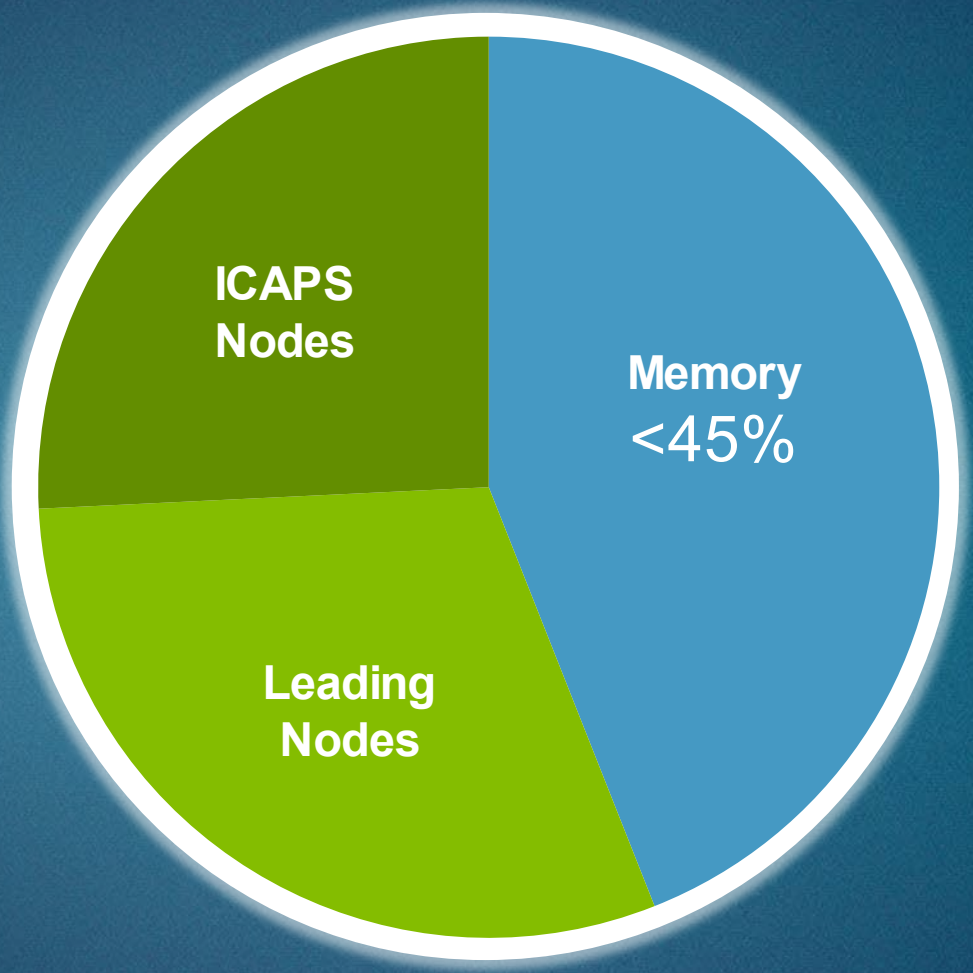
President and CEO
Sony Semiconductor Solutions Corporation

> *Image sensors with AI functionality are going to change how we engage with the world around us. At the heart of this is Sony's CMOS sensor, where innovations in process technologies are required to improve performance attributes such as sensitivity, resolution and dynamic range.* ***Applied Materials has created new materials solutions that are co-optimized with their broad equipment portfolio, which allows Sony to continue to improve image sensor capabilities.***

WFE Mix



10-Year Average



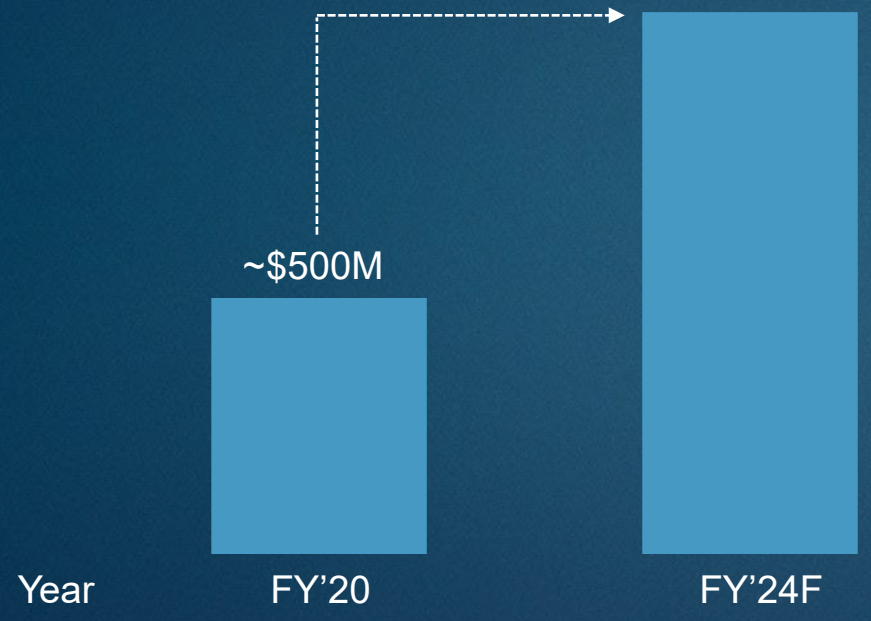
2018-2021e

= memory, = foundry-logic

Source: Gartner, VLSI, Applied Materials

Positioned for Growth in Packaging

Early innings of multi-year growth



Packaging revenue >$800M in FY'21

#1 in bond pad, bump and TSV

Broad product portfolio + full-flow lab

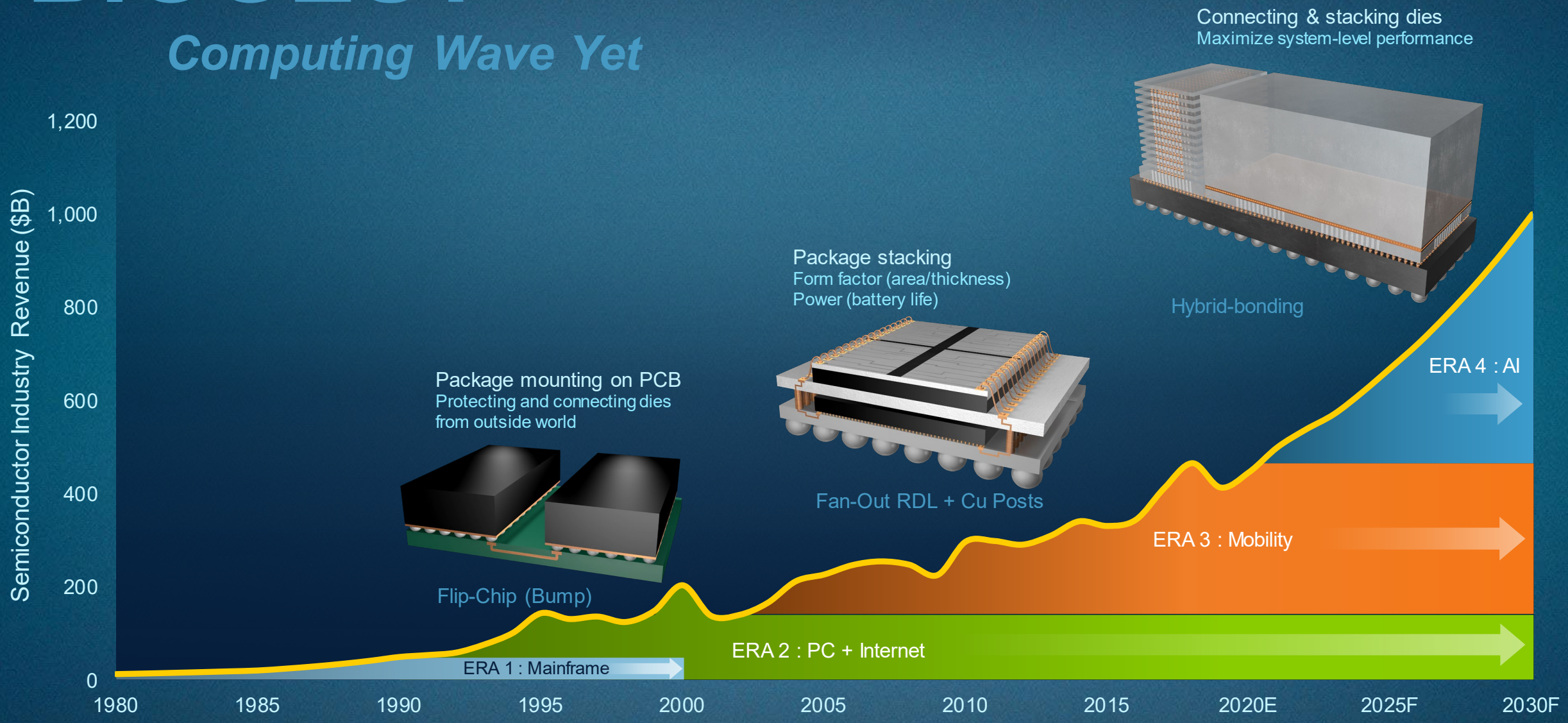
Key eco-system partnerships

Delivering system level PPACt gains
↓ R, ↓ power, ↓ area, ↑ performance

TSV = Through-Silicon Via

BIGGEST

Computing Wave Yet



Source: SEMI, VLSI, Applied Materials

TAKEAWAY
Messages

1. ICAPS markets fuel data generation at the edge and demand for leading-edge logic and memory in the cloud
2. Advanced packaging enables the PPACt™ benefits associated with Moore's Law to continue
3. Applied's unique portfolio breadth enables outperformance in ICAPS and advanced packaging

* Non-GAAP adjusted EPS