ICAPS & PACKAGING MASTER CLASS

PREPARED REMARKS | SEPTEMBER 8, 2021

APPLIED MATERIALS

MICHAEL SULLIVAN | Corporate Vice President, Investor Relations

Hello everyone. I'm Mike Sullivan, head of investor relations at Applied Materials, and I'm pleased to welcome you to the third event in our Master Class series.

Today we'll cover two topics. One: the ICAPS portion of the foundry-logic market. As a reminder, ICAPS stands for IoT, communications, automotive, power and sensors. And two: heterogeneous design and advanced packaging. On the events page of our website you can find a copy of today's slides, speaker bios, our prepared remarks, and our news releases and blogs. The fourth Master Class is targeted for October 18 when we'll cover process control and process recipe optimization using our new AI^{X}™ platform.

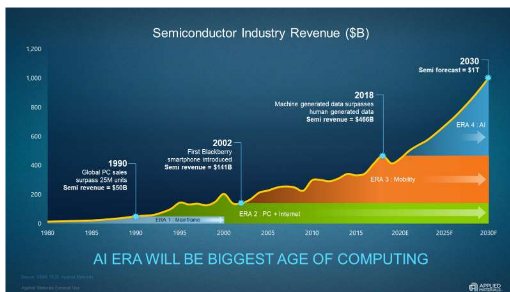
Here's today's agenda. In a moment, I'll give you an update on our foundry-logic growth thesis and how the Internet of Things plays an enabling role. Then we'll have a fireside chat with Dr. Tom Caulfield, CEO of GlobalFoundries. Next, Dr. Sundar Ramamurthy will introduce you to the ICAPS and advanced packaging markets and the approaches we're taking as a company.

Sundar will introduce Dr. Mike Chudzik, who will detail major technology inflections in the ICAPS markets, and Dr. Nirmalya Maity, who will show you how packaging is rapidly evolving to accelerate PPACt™ for semiconductor and systems companies. After the technology sessions, Sundar will summarize the ICAPS and packaging growth opportunities for Applied, and then he and Nirmalya will both be available to take your questions. We plan to finish between 10:30 and 11:00 Pacific Time.

TAKEAWAY
Messages

1. ICAPS markets fuel data generation at the edge and demand for leading-edge logic and memory in the cloud
2. Advanced packaging enables the PPACt™ benefits associated with Moore's Law to continue
3. Applied's unique portfolio breadth enables outperformance in ICAPS and advanced packaging

There are three headlines for today's Master Class. One: the ICAPS equipment market has grown significantly over the past four years and is now more balanced with the leading nodes. The ICAPS markets are fueling data generation and the need for leading-edge logic and memory. Two: packaging is no longer an afterthought. Heterogeneous design based on chiplets is the future of semiconductors and computing. Advanced packaging enables higher performance and lower power. It also enables area and cost savings and faster time to market. Three: Applied is using its unique breadth and depth to accelerate technology solutions for the ICAPS and packaging markets, and we expect this to generate billions in annualized revenue growth in 2024 and beyond.



Now I'll take a moment to connect the ICAPS markets to our data thesis. The next handful of slides will be familiar to you if you attended our investor meeting in April. We believe that in 2018 we entered the fourth era of computing where the Internet of Things, Big Data and AI are creating a new wave of growth, complementing the markets for PCs and smartphones.

2018 also marked the transition from an app-centric world, focused on people using applications, to a data-centric world, where machines generate more data than people do. By 2025, we expect machines to generate 99 percent of the data created each year. This means the growth of computing is no longer gated by what people do with digital devices like PCs and smartphones.

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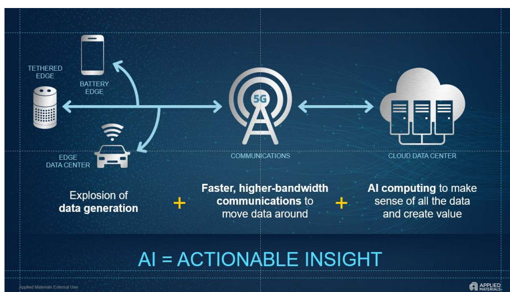
And the biggest of the data-centric applications is the "I" in ICAPS, the Internet of Things. We see the industrial IoT category being far larger than the home IoT category, and this is what we mean about the fourth era of computing and industry 4.0 being non-consumer discretionary.



The ICAPS markets are heavily responsible for what happens on the left side and the middle of this chart. IoT devices on the edge will generate the data and communication silicon will help route the data to the cloud. On the right side, the cloud data centers will use leading-edge logic and memory to make sense of the data using AI. This sets up a virtuous cycle for semiconductors whereby the ICAPS semiconductor markets fuel the markets for leading-edge logic and memory. At the bottom, the economic value that comes from the actionable insights generated by AI helps to fund the build-out of this ecosystem.

Semi content per unit	2015	2020	2025F
HIGH END SMARTPHONE	$100	$170	$275
AUTO (GLOBAL AVERAGE)	$310	$460	$690
DATACENTER SERVER (CPU + ACCELERATOR)	$1,620	$2,810	$5,600
SMARTHOME (GLOBAL AVERAGE)	$2	$4	$9

SILICON CONTENT GROWING AS EVERYTHING GETS SMARTER

As you'll see in today's class, as the fourth era of competing takes hold, Silicon content is growing in all kinds of devices, from the edge to the cloud. We'll go into the details about ICAPS silicon in smartphones and cars, for example, and in cars, how all of the ICAPS categories come into play, notably new power chips that are disrupting the transportation industry.

And this means the fourth era of computing is fueling growth for the semiconductor industry. Third-party researchers believe semiconductor revenue could reach a trillion dollars in the 2030 timeframe. If they're right and if equipment capital intensity is about 15 percent then as it has been recently, then the semi equipment industry could be on its way to around $150 billion with compound growth in the mid to high single digits.

Finally, what will the equipment spending mix be? Based on the historical mix, memory will account for less than 45 percent and foundry-logic will be over 55 percent. Using a rolling 10-year average, about two-thirds of foundry-logic would be on the leading edge and around one-third would be on trailing nodes. But that view deserves an update. We talked about how computing changed beginning in 2018 and Sundar will show you how the foundry-logic mix has changed as well.

Finally, we're retiring the term "trailing nodes" because it's a disservice to all the growth and the innovation that's happening in the non-single digit nodes. The new name is ICAPS. And that brings us to our fireside chat with Dr. Tom Caulfield. We can't think of a person more qualified to talk to us about the growth of the ICAPS market. Tom's complete bio is on the event website.

What I'd like to highlight for the Master Class is that Tom holds a degree in physics and three degrees in material science and engineering, including his Ph.D. He's applied his knowledge in a wide range of industry leadership capacities, spanning semiconductor process technology ramps, fab management at IBM and GlobalFoundries, and even semiconductor equipment company leadership.

Today he's the CEO of one of the world's most important semiconductor manufacturers. Tom tremendously strengthened GlobalFoundries' position in the industry by focusing the company on the two-thirds or greater portion of the end market that Applied calls ICAPS.

Tom, thank you for joining us.

THOMAS CAULFIELD | Chief Executive Officer, GlobalFoundries

Thank you Mike, and to Gary too, for having me here today and be able to participate.

Mike Sullivan: ***Tom, given your unique position in the industry as the CEO of one of the most diversified foundry semiconductor manufacturers, can you give our audience your view on how the industry got to where it is right now? Every day we hear about the chip shortage and just recently major automotive companies like Ford, GM and Toyota idled their plants and furloughed thousands of employees. What's your perspective?***

Yeah, it's amazing. We're an industry that's pretty much changed the world and we're starting to get more recognition for when we don't do enough of what we do. We were in the press every day. I give this a lot of thought. And for me, this is a decade-and-a-half in the making. We had different golden ages in the semiconductor industry. It started first with PCs and then it went to networking and then mobility at the turn of the century. And then about 2009, we hit probably the "motherload" as an industry, the advent of the smartphone and it's accelerated the next golden age of our industry. And so, for me, this intersection of a supply-demand imbalance was always in the making and potentially accelerated by two to three years because of COVID-19.

I think what happened was the digital transformation was going on for a long period of time in a revolutionary way of deployment. But as humans, we only adopted it in an evolutionary way. We would never have done this remotely. I would have been sitting next to you in a studio. I would have been at your event. And we suddenly discovered the power of the digital universe we live in. And now instead of pushing technology, people were pulling it. And what it did is -- this intersection of supply-demand imbalance -- it pulled that in by two to three years. As a result, the offset is that much more severe and that's where we are today.

Mike Sullivan: ***Tom, it's been almost three years since you led the strategic pivot for GF making the decision to focus the company on the many opportunities that do not include the single-digit nodes. How much of the market are you serving and why are these markets strategic?***

Think about the same decade and a half, the advent of the smartphone was about the same time GF was born in 2009 and the industry really shifted. We went with this same movement. We went from a compute-centric industry to a pervasive deployment of semiconductors. In that same period of time, the birth of GF in 2009 to where we made that pivot, the industry went to where 74 percent roughly is being served by 12 nanometers and above, and single digit nodes make up the balance. And so we started to look at where we were successful as a company and where we were struggling. Given our scale, given being a second, third source and the kind of investments required to be in single-digit nanometer was really counter to where we can be valuable to the industry, our customers and to ourselves as a business.

We made this pivot to go after that 74 percent where we had great demonstrations of creating platforms on our different nodes. Singapore, our FAB 7 facility, had been doing this for almost a decade. We had a broad customer base and a broad set of end markets we were serving. We said, look, we can play a much more vital role in this industry instead of being a me-too in single-digit nanometer, let's go become number one or number two in the end markets where we can create real value and differentiation for our customers. Let's make the rest of the company look like our Singapore FAB 7 facility at the time. And that was the journey we embarked on in 2018.

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Mike Sullivan: ***So, Tom as a follow-up, people sometimes think the non-single-digit nodes are "legacy nodes," or "trailing nodes," and they don't think about opportunities to continue to further innovate. Do you see opportunities for things like new materials, new device architectures beyond the single-digit nodes?***

Yeah, Mike. They're going to believe I fed you this question. This idea that as an industry, because of the complexity, I believe we don't do a really good job of explaining ourselves. We try to capture innovation in a sound bite. Oh, it's the size of the transistor that's scaling. Quite honestly, I find it insulting to the tens of thousands of engineers across many companies that innovate every day on platforms. We create embedded memory for secure transactions. If you go to a grocery store or any store and you do Google Pay or Apple Pay, it's on a chip we make. And look what it does; it makes sure we do a transaction touchless and secure. I don't call that legacy. I call that awesome. So, I think innovation takes many forms in our industry. It's a very complex industry. We choose to innovate and create features on nodes – high voltage, low voltage, BiCMOS devices – we could do battery management, we can do high voltage for display. That's how we innovate. And we constantly spend our R&D dollars focused on where to make those new materials, new capabilities, different transistors, the different IP that allows us to create solutions very targeted to end markets.

Mike Sullivan: ***Tom, Applied agrees with you on the non-single-digit nodes being really important. And so, we did form this group called ICAPS to better address the market. In order for you and your customers to be successful in the end markets you're now playing in, what are you looking for, including from equipment partners like Applied?***

So if I take a step back, when we took the pivot in 2018 as a company, we had to retool ourselves in understanding not only our go-to-market strategy, but what were the tools we needed and the personnel we needed. We went out and got industry experts in the end markets we wanted to play in, so we knew where to focus our R&D dollars and we knew how to better engage with our customers. I think we've gotten to a point now in the maturation of GF and our journey in this pivot where we need to start to bring in the equipment suppliers in a more deep and holistic way, so that they can spend their R&D dollars to support the features we're looking to build upon in our technology solutions.

Mike Sullivan: ***So, Tom, when you think about your business and your end customers, what are the opportunities that the equipment companies have?***

Back to this idea of pervasive computing is about creating features on platforms. I think it's a real opportunity for the equipment industry. Remember I came from Novellus so I knew how the game was played. You tried to get a new position with every new node as scaling was taking place. If you lost at 28nm, you tried to win it again at 14nm. Well, here's an opportunity as we start to add capacity or re-add capacity into these nodes that create platforms. It's an opportunity with the right investments and partnerships to re-win or re-establish positions that you might've lost in the beginning. It's an opportunity to use innovation and R&D to win where CapEx is going to have to be spent to create more capacity in these areas.

Mike Sullivan: ***Finally, Tom, what didn't I ask you today that I should have?***

When you change a strategy, it's a little bit about transformation and strategy. We started where we had four business units that were technology centered – FinFET, RF, FDX and then a catch-all in CMOS. And the problem with that was we don't sell technologies, we sell solutions. We thought about if we're going to be a foundry of choice to go get single-source business, where our customers see value in the

differentiation we could provide. We needed to have a business unit that understood end markets. We needed to retool the company, the whole commercial engine. And we went out and found the very best leadership team in these end markets we wanted to serve – mobility, compute, Internet of Things, automotive – and we brought them into the company so they could lead our efforts in understanding what the total solution needed to be. I think Gary [Dickerson's] biggest claim to fame is he understood markets. He understood how to position a company to understand what is important to get done, to go win in the marketplace. And a little bit of what GF did in our transformation is to take that playbook. Figure out how we're going to be successful. How do we organize our commercial engine? It started with deep industry understanding of the markets we're going to play in, and then leveraging the expertise we bring in with deep customer partnerships to create the business we have today that's predominantly single-source business.

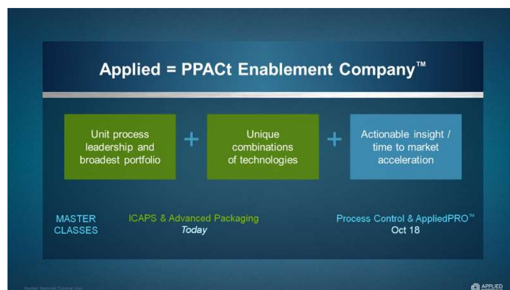
Mike Sullivan: ***Well that's exactly what we're trying to do* with *our ICAPS group, Tom. So, thank you so much for joining us today. We really appreciate it.***

I appreciate you having me here, Mike.

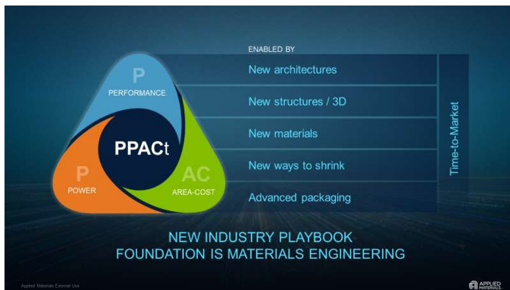
Mike Sullivan: ***And now Sundar, it's over to you.***

SUNDAR RAMAMURTHY | Group Vice President, Epitaxy, Packaging & ICAPS

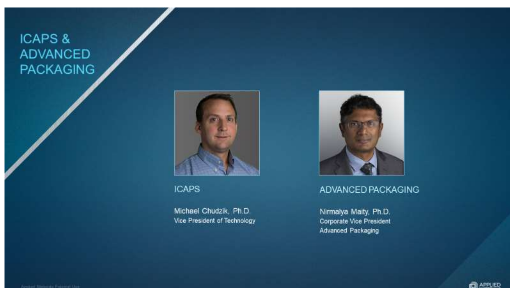
Thank you, Mike. Hi, I am Sundar Ramamurthy, General Manager for the ICAPS and Packaging businesses at Applied. I will introduce you to today's Master Class presenters and set the context for these businesses on how they fit Applied's overall growth strategy.



You may know that Applied's goal is to be the PPACt enablement company for our customers. We are investing to drive the new playbook for PPACt with our unique portfolio breadth in unit process technologies and by combining our technologies in unique ways, using both co-optimization and integration of adjacent process steps. In our next event on October 18, we will discuss another of our strategies, which is accelerating process development and ramps using our AI^x platform technologies.

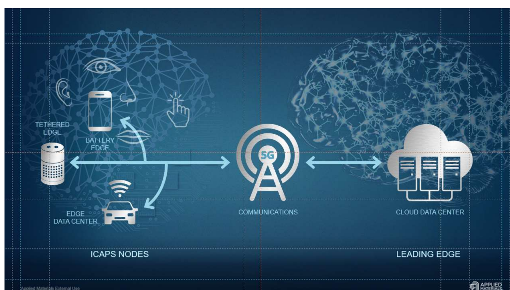


The new playbook for PPACt has five elements that are all driven by materials engineering. In the cloud, it's all about new architectures and advanced packaging, which are number one and number five in the new playbook. At the edge, it's about designing intelligence into all kinds of devices as Tom Caulfield discussed earlier, using all of the ICAPS nodes. New materials is number three in the new playbook. The entire automotive industry is being transformed by new materials like silicon carbide.



In today's classes, the ICAPS technologies will be covered by Dr. Mike Chudzik, who is Vice President of Technology at Applied and one of our top materials and device experts. Mike Chudzik presented at the Logic Master Class and today, he's primarily focused on inflections in the ICAPS markets. He received his Ph.D. in electrical and computer engineering from Northwestern University. He joined Applied seven years ago and was at IBM for nearly 14 years before that.

Heterogeneous design and advanced packaging will be covered by Dr. Nirmalya Maity, who is Corporate Vice President and Head of our Advanced Packaging business. Nirmalya earned his Ph.D. in chemical engineering from Cornell University and has over 25 years of experience developing semiconductor materials and equipment solutions. Now I'll give you my perspective on how these businesses fit within the industry and within Applied. The previous Master Classes focused on memory and advanced logic, all of which are on the leading nodes of technology. Think of these as the brains of the most powerful computers.



But to digitize the world around us and create the Internet of Things, we need more than powerful brains. As humans, we sense the world with our eyes, ears, noses and skin. And we rely on analog-to-digital circuitry to interface with computers. The ICAPS technologies are the equivalent of these, making the digital future possible. A smartphone without ICAPS is just a calculator. Without ICAPS, there are no autonomous vehicles. There is as much innovation in ICAPS as anywhere else in computing, and there is certainly as much growth. Packaging is another term that understates a valuable change happening in our industry. Heterogeneous design and advanced packaging are enabling us to continue delivering the benefits of Moore's Law in a manner that's the polar opposite of what Moore's Law stands for in most people's minds.

Applied has a common strategy in both ICAPS and packaging. You may recognize this slide from our investor meeting. Both ICAPS and packaging are solutions businesses. Our teams are focused on the end markets, working with the leading customers to create innovations based on the full portfolio of Applied Materials, including co-optimized and integrated solutions. Nirmalya will explain how we are doing this in packaging. The ICAPS markets are diverse. The biggest equipment opportunity is related to the “I” in ICAPS, which stands for IoT.

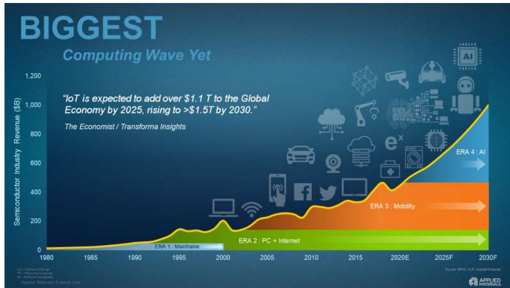
It's general-purpose logic across a wide variety of nodes. The next biggest equipment markets are the “P” and “S” in ICAPS, power chips and sensors. Notably, CMOS image sensors. Mike will give you insights into the technology inflections in those markets. The “C” in ICAPS, communications, is critically important because it's the glue that binds the digital world. And finally, the “A” in ICAPS stands for automotive. No other market makes as much use of the full variety of ICAPS technologies and the biggest inflection in automotive is electric powertrains. And those are also enabled by ICAPS. That brings us to one of our announcements. Today, we introduced new innovations in our ion implant and CMP portfolios.

These products are specially designed to help our ICAPS customers take silicon carbide to larger 200-millimeter wafers. This will enable them to increase output for the burgeoning demand ahead.

Our ICAPS team is excited to be working more closely than we ever have with companies that are at the forefront of these markets. We are excited about helping enable the electrification of the global transportation industry. Now, for more insights into the ICAPS inflections, I'll hand the meeting over to Mike Chudzik.

MICHAEL CHUDZIK | Vice President, Technology

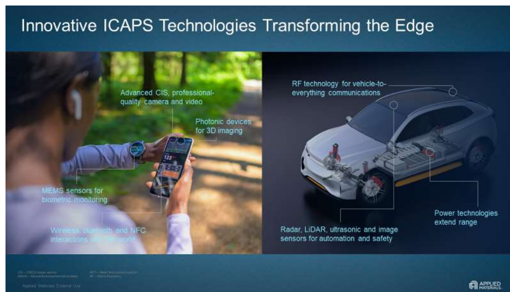
Thank you Sundar.



Hi, I'm Mike Chudzik, and it's nice to be joining you again. I believe that we're in the early innings of the next big compute wave characterized by the massive growth of Big Data, artificial intelligence and new Internet of Things devices. These devices are expected to add over a trillion dollars to the economy over the next four years and are largely enabled by ICAPS nodes and technologies.

The end markets for this next era in computing are driven by a mega-trend of connected devices at the edge, and the world's largest companies are investing to win. The edge includes multi-billion-dollar markets like AR/VR, automotive, mobile computing and communications, industrial and home IoT, wearables, and healthcare. The competition is about differentiated devices that provide user benefits derived from PPACt. Whether commercial or consumer, we all want devices with the best performance, lowest power for longer battery life, smaller area for size and weight, and all at the lowest possible cost.

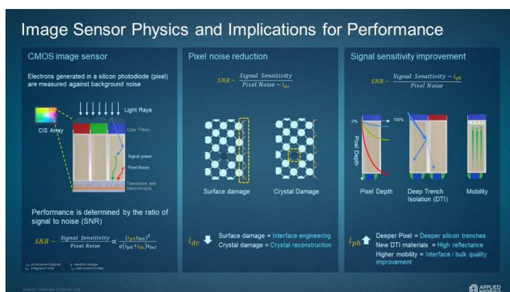
Time to market will determine who gains and who loses share. At the heart of these new connected devices are ICAPS technologies, including IoT embedded processors, RF communication chips, power modules and CMOS image sensors. Along with MEMS devices, photonics chips and a whole host of specialty components that help our devices sense the analog world, compute locally or in the cloud, and translate information back to us using analog sensors. Increasingly, the data generation, processing, and even the decisions and physical actuations will be machine-to-machine with no humans in the loop.



To get a sense of the size and value of the ICAPS markets, let's take a look inside a few of the more recognizable end-use applications – smartphones, wearables and electric vehicles. The smartphone has over 120 chips, and over 70 percent are specialty devices. For example, there are multiple CMOS image sensors and photonics devices for ambient light sensing, facial recognition and a form of radar called lidar.

There are power devices to deal with everything from battery management to power regulation. Smartphones, and even many wearables, contain a variety of RF technologies to enable communications over the networking technologies deployed around the world. And there are MEMS devices, including microphones, fingerprint sensors, accelerometers, gyroscopes and pressure sensors. The latest electrical vehicles hitting the market are often described as smartphones on wheels. The analogy works. Consider the power electronics needed for car battery charge and control, and the RF needed for car-to-driver, car-to-car and car-to-cloud communications, as well as the sensors needed for navigation and safety, which span ultrasonics, radar, image sensors and lidar.

Applied Materials formed the ICAPS engineering and customer support team to enable innovation across ICAPS nodes and help customers in these end markets accelerate and advance their technology roadmaps. The ICAPS team allows for customers to be more focused on their markets than in technology integration. And the closer we work with ICAPS customers, the more we can help not only address their near-term challenges, but also use new materials and materials engineering approaches to solve really tough long-term challenges. Now let's get more technical and take a closer look at two important examples. I'll cover CMOS image sensors in depth, and then turn our attention to electric vehicles.

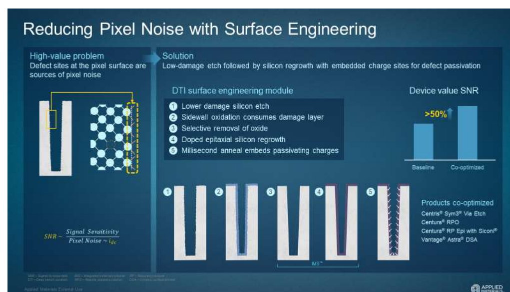


CMOS image sensors are one of the largest ICAPS market segments. They are a key ingredient to most edge devices with at least one found in everything from cell phones to smart cars, smart factory equipment and of course, even doorbells. A CMOS image sensor array is arranged into millions of individual light sensitive pixels for blue, green and red. Each pixel is formed by etching a deep trench into silicon.

The structure collects light rays that enter through a micro lens and color filter and when photons interact with the electrons in a silicon atom, free electrons are created. The freed electrons are registered as a light signal by the readout circuitry. The performance of each of the pixels is determined by the signal to noise ratio of the device. The input signal sensitivity is dominated by the photocurrent or i_{ph} current, which is generated by incident light as shown on the top line of the equation.

Pixel noise is on the bottom line of the equation. It usually consists of three parts: pixel noise, readout noise and noise variation. Dark current or i_{dc} is the main contributor to pixel noise. Dark noise occurs when loosely bound electrons escape from the interface between the pixel and isolation region, and it can be reduced by improving the crystalline and interface qualities.

Light sensitivity depends on a few key factors. First, the depth of the pixel. Deeper pixels give the incoming light rays more opportunity to hit an electron inside the pixel and generate a signal. Second, higher mobility which increases the probability of registering the incoming signal. And third, the reflectivity of the isolation that separates each pixel. Higher reflectivity improves the ability to focus and capture the incoming light rays and prevents them from passing through to a neighboring pixel, which creates signal loss. Improving CMOS image sensor performance is a classic materials engineering problem that falls within the expertise of Applied Materials.



Optimizing unit process steps in the image sensor module or, better yet, integrating the steps can significantly reduce pixel noise. In fact, the pixel noise can be dramatically reduced by optimizing the pixel's deep trench with surface engineering. The materials engineering includes several closely linked process steps in the deep trench isolation module. Currently deep pixel isolation calls for trench depths of six to 10 microns with aspect ratios of at least 60:1 and a roadmap target of 100:1. Low light sensitive applications depend on deep pixel technologies, so high aspect ratio pixel isolation is critical.

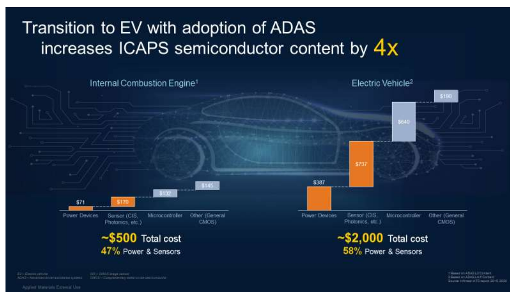
We are working to deliver the required high aspect ratios with minimal sidewall roughness using Applied's latest 300-millimeter reactive ion etch tool, the Sym3®. After etching, the surface is cleaned and the sidewall surfaces are passivated. Defect-free, smooth trench sidewalls are critical to ensuring the lowest surface defect density possible, which ensures that loosely bound electrons are not released from the trench to pixel interface, which would cause unwanted signal noise at the pixel level.

Applied Centura® RPO chamber is used to create a conformal oxide layer along this trench sidewall that is just several nanometers thick. This layer converts nanometers-size surface bump defects to an oxide layer. In a subsequent step, that oxide layer is removed, leaving a smooth silicon trench sidewall. In fact, the oxide layer is selectively removed under high vacuum and combined with a high-concentration epitaxial silicon boron layer, which produces pristine surfaces that are free of damage and defects which are key to reducing signal noise.

This process takes place in Applied's Centura® RP Epi system with integrated Siconi® pre-clean chamber. The combination of these co-optimized and integrated solutions results in a 50 percent increase in the signal-to-noise ratio. The high-quality, deep trench isolation sidewalls also produce a similar reduction in dark current.

Integrated solutions can also improve signal sensitivity. We've even introduced an advanced light isolation material for the trench reflector which confines the light signals. The industry has made progress with the tungsten layer which improves trench isolation by blocking light but doesn't serve as a good reflector. The next inflection is a new trench material with a highly reflective aluminum layer.

This new inflection demands a process sequence that includes applying a novel conformal liner material followed by the deposition of aluminum using CVD. The liner and the aluminum layers are highly conformal and have reflectance properties tuned to maximize the reflected light. This module is then followed up by a co-optimized aluminum CMP process. Combining the conformal and void-free CVD process with the highly reflective aluminum metal and liner produces filled structures that boost quantum efficiency by more than 2X. Applied's conformal CVD aluminum and CMP are key to this performance.



Now let's shift gears and take a look at a major inflection in the automotive market where internal combustion engine or ICE cars are getting more sophisticated even as electric vehicles become mainstream. Even ICE vehicles have a staggering number of chips, and 47 percent of them are specialty power and sensor devices with unique performance requirements due to the extreme operating ranges. But, electric vehicles have almost twice the semiconductor content measured in dollars.

And by 2030, we expect the semiconductor content to double again, as car makers enable successively higher levels of advanced driver assistance systems or ADAS features. Level four and five vehicles will continue to increase demand for ICAPS specialty technologies, such as MEMS, lidar, CMOS image sensors, radar, ultrasonics and RF. In the transition from ICE to EV, the biggest growth will be in next-

generation power devices that handle everything from power distribution to battery charging acceleration. Silicon carbide MOSFET chips are growing particularly quickly as electric vehicles adopt higher voltages.

These chips switch voltages up to six kilovolts with current in the hundreds of amps. The unique material properties of silicon carbide include a wide band gap and fast charge transfer. As a result, silicon carbide chips switch more efficiently than silicon-based high-power chips and dissipate less power. From an engineering perspective, the power dissipation of a silicon carbide chip is governed by the square of the drain current, I_D, and the on resistance, R_{ON}. To improve the efficiency, we reduce the on resistance by increasing the electron mobility.

For a perfect crystal, electron mobility can be improved with gate orientation and cell pitch reduction and is inversely proportional to doping concentration. Defects in the silicon carbide crystal created during the manufacturing process degrade mobility, which increases electrical resistance, reduces performance and wastes power. Two of the key process technologies are silicon carbide wafer CMP which reduces surface defects, and ion implantation which optimizes electron mobility by reducing bulk defects in the silicon carbide.

Power chip formation begins with a bare silicon carbide wafer that needs to be polished smooth because it's the base upon which a subsequent epi layer is grown. Silicon carbide is a very hard material, much harder than materials like silicon, silicon dioxide and copper that are commonly planarized with CMP technologies. At the same time, a silicon carbide chip needs to have a uniform crystalline lattice throughout the device. There are two images near the center of this slide. The image on the top shows a wafer in the condition typically received by the manufacturer. There's a high concentration of scratches from the grinding process used to produce the wafer.

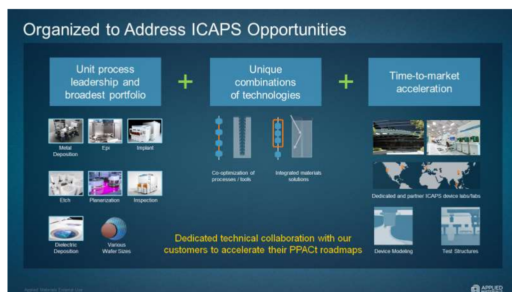
Growing a silicon carbide epi layer on top of this surface would create dislocations and defects in the crystalline lattice. The image on the bottom shows the dramatic improvement in surface quality that can be achieved with optimized chemical mechanical polishing. Applied is introducing a new CMP tool called MIRRA® Durum™ which is optimized for planarizing 150-millimeter and 200-millimeter silicon carbide

wafers. It integrates material removal measurement along with cleaning and drying steps, and it provides a 3X improvement in surface quality, as well as a 3X improvement in the material removal rate.

A second key process technology is ion implantation. Precisely injecting negatively and positively charged ions in specific regions of the lattice creates the active region that controls the flow of high currents. Implanting ions in silicon carbide wafers and diffusing them in the material is much more challenging than in silicon wafers.

The dense crystalline structure and extreme hardness of silicon carbide make it practically impossible to diffuse the ions. Implanting high doses at high energy helps, but at standard clean room temperature, the implant processes actually destroys the crystalline lattice. Applied is introducing a new hot implant technology that uses 500-degree-Celsius temperature and medium-current energy to inject ions without severely disrupting the lattice, thereby maximizing electron mobility efficiency.

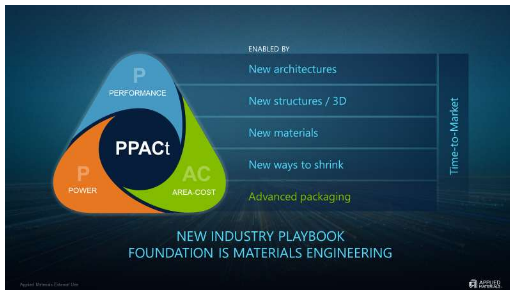
The new VIISta® 900 3D silicon carbide system is a high productivity, low cost of ownership solution. On the slide, we compare two types of aluminum ion implantation, one at room temperature and the other at 500 degrees Celsius. On the left, you can see damage to the crystalline surface with some areas becoming amorphous, whereas in the right side image, a hot implant preserves the crystalline structure. The bar chart on the right shows that our new approach reduces resistivity by over 40 times.



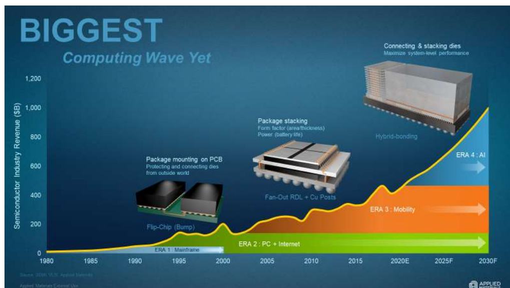
These advances in materials engineering for CMOS image sensors and silicon carbide chips are just two of dozens we are working on for the high-growth ICAPS applications together with leading customers throughout North America, Europe and Asia. Our customers are excited about the ICAPS group, which includes device teams focused on unit processes across a variety of wafer sizes, along with process co-optimization and integrated module innovation. And now I'd like to hand the meeting over to another one of my colleagues, Dr. Nirmalya Maity.

NIRMALYA MAITY | Corporate Vice President, Advanced Packaging

Thank you, Mike.

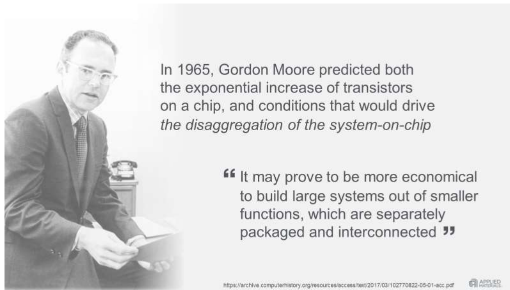


As we have communicated in several forums, at Applied we believe that driving further improvements in power, performance, area, cost and time to market requires a new playbook. As I will describe today, advanced packaging is a very powerful tool in this new playbook. All around us customers are introducing heterogeneous designs, where as many as dozens of chiplets and devices are being integrated as one. Applied is already enabling and growing with this trend, and we are committed to helping our customers take this even further.

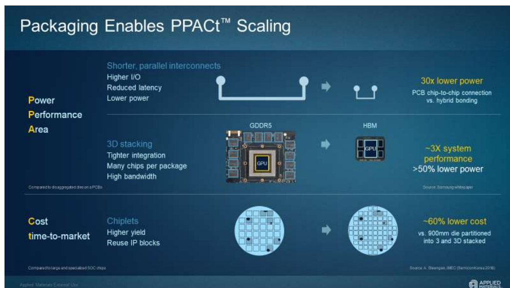


Packaging was historically about protecting the die and connecting it to the PCB. It was a commodity low-value part of the industry, but that's rapidly changing. As we have moved from the PC era to the mobile era to the fourth wave of computing, packaging has evolved substantially. Today, advanced packaging using wafer fab equipment technologies allows the industry to stack and connect multiple logic memory and specialty chiplets to optimize the system for higher performance, lower power consumption and smaller area and lower costs.

This newfound flexibility is also being used to speed time to market. It's a competitive imperative for the world's leading semiconductor and systems companies. Until recently, the industry was focused on monolithic integration, putting as many logic and memory blocks as possible onto a single die. It worked like clockwork for decades and as it did, lithographic 2D scaling of transistors and interconnect wiring was the key to reducing costs. But today, the industry has a major challenge because two exponentials are at odds. Data is still growing exponentially while intrinsic 2D scaling is not.

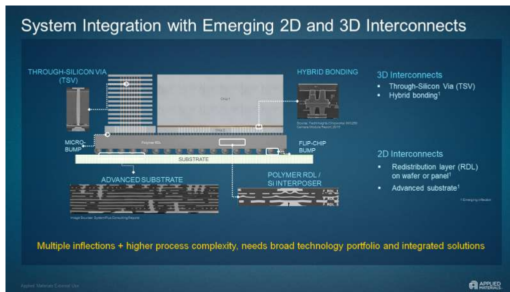


As a result, in the AI era, designers can't get all of the circuits they want into a single die anymore. And with the high cost of shrinking on the leading edge, the cost reductions aren't happening at the traditional rate either. Heterogeneous design and advanced packaging create an alternate way of continuing the benefits associated with Moore's Law. Now we will focus on how advanced packaging delivers PPACt attributes and how Applied solutions directly contribute to that.

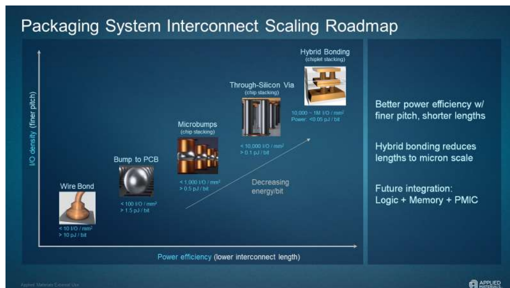


Let's examine how advanced packaging enables PPACt at the system level. First, we will consider how to improve PPA: power, performance and area. The conventional approach was assembling individually packaged die on a printed circuit board (PCB), and then connecting them with wiring. Advanced packaging enables us to bring unpackaged dies together in an advanced package that uses much shorter 2D and 3D connections.

This approach delivers high data bandwidth and much lower power consumption. It also allows us to pack more transistors in a unit area. So, it delivers clear PPA benefits as compared to using a PCB. Let's also consider how we can reduce cost and time to market. Monolithic designs result in large dies that are expensive to design and tape out. And the larger the die, the lower the yield. Heterogeneous design lets us disaggregate the design into smaller chiplets which can be connected in a high-performance package. Proven IP chiplets can be reused. This design and mix-and-match flexibility can save cost and time to market. Advanced packaging allows us to combine disparate logic, memory and specialty devices like power and sensor components, to deliver optimized system performance and unique capabilities.



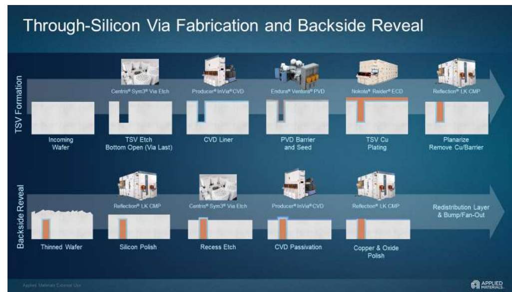
The architecture on the left represents how this can be accomplished. Here, multiple DRAMs are stacked and connected to a logic die stack. The 3D memory stacks and the logic stacks are connected using dense 2D connections incorporated into silicon interposers and advanced substrates. In the future, we will achieve significantly greater PPACt benefits using heterogeneous integration technologies that we are now developing together with our customers and partners.



Advanced packaging gives us many architectural options. At the core, however, are a few basic chip-to-chip interconnect building blocks shown here. Each successive technology offers higher input-output density, as well as lower power consumption per bit of data transfer. Applied Materials has the equipment industry's number one position across today's existing technologies, which include bump to PCB, micro-bumping of stacked chips and through silicon vias. We're working with our customers and partners to accelerate an emerging technology called hybrid bonding that will allow chips to be directly combined with copper-to-copper bonding without the need for micro-bumps. Next, let's examine how these building blocks can be put to use with memory packaging as an example.

As DRAMs moved to advanced packaging schemes like flip-chip and stacking, our aluminum bond pad, redistribution layers and bumping technologies are the industry standard way of implementing these schemes. We have decades of experience designing aluminum deposition processes with the optimal film and defectivity properties. This translates to a high share in a growing market. Computing applications

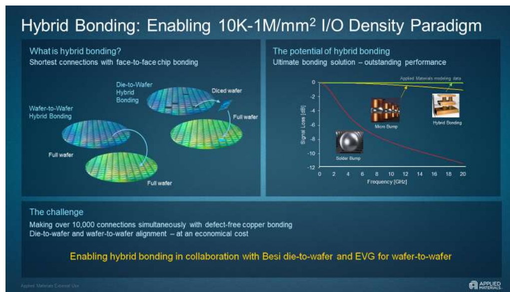
like AI accelerators need even more die stacked and higher bandwidth. Through silicon vias can be used to stack and interconnect 8, 12 and, in the future, even 16 DRAMs. These techniques are in high-volume production and our annual revenue is in the hundreds of millions. Now let's examine the through silicon via approach and the steps needed in a co-optimized process scheme.



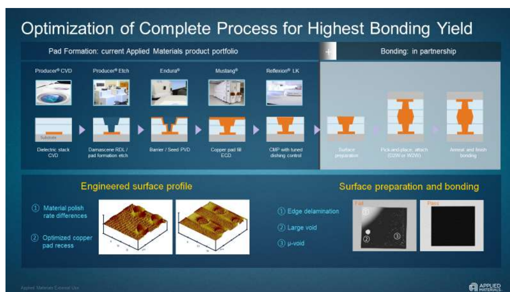
As you can see, the TSV process involves creating a deep via in the silicon from the top of the wafer followed by a reveal process that exposes the backside of the wafer. Applied already has a line of industry-leading products and processes for back-end-of-line interconnect steps. We have developed derivatives of these products to serve the TSV packaging market, and we have high share. It took some time for TSV to reach high volume. Engineers were concerned about the cost involved with these extra steps. But today the economics of chip stacking using TSV are very clear, especially when compared to the rising cost of intrinsic 2D scaling.

To enable further scaling using TSV, we need smaller vias which create higher aspect ratios. To help customers overcome the technical challenges, we are developing co-optimized solutions. We have developed a TSV etch process, which produces a very deep, high aspect ratio silicon etch with a smooth via profile. We then deposit a highly uniform dielectric liner. This liner has also been optimized for low temperature deposition, which is needed for integration without exceeding the overall terminal budget.

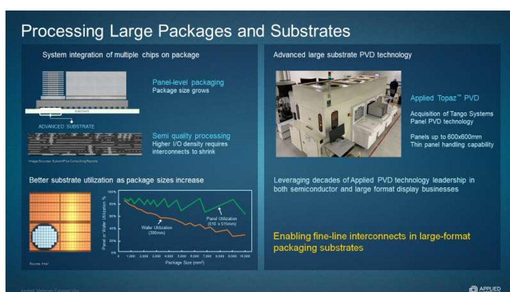
Our film also has the optimal density for high electrical performance and reliability. The smaller vias and higher aspect ratio also make the metallization process more challenging. To help our customers, we are co-optimizing across multiple processes, including copper PVD, copper electroplating and CMP. These unique solutions are resulting in process tool of record positions in some of today's most advanced logic designs, which will enable us to generate significant revenue over our model horizon. As we think ahead to further breakthroughs in I/O density and power per bit, the next logical step is direct chip-to-chip bonding.



The graph on the right shows that packaging elements like bumps and micro-bumps can have a negative impact on signal integrity. Copper-to-copper hybrid bonding will allow us to achieve performance that is very close to monolithic designs, with almost no power and signal penalties. The technology challenge is achieving defect-free copper-to-copper bonding with almost zero die-to-die alignment errors, all at an economic cost. To help do this, we have created a development partnership with a company called Besi, a leader in pick-and-place and bonding technology. We also recently signed a joint development agreement with a company called EVG, which is designed to help us accelerate wafer-to-wafer hybrid bonding technology. Achieving the highest yielding chip-to-wafer hybrid bonding process requires multiple steps to be co-optimized.



For example, the surfaces to be bonded need to be prepared in a way that produces a particular microstructure and topography. We achieve this by optimizing the metallization and the planarization processes as shown on the bottom left graph. Applied Materials has the equipment solutions to enable this, including a CMP process with integrated sensors. Process knowledge is also key to providing chemical surface activation and managing queue times. Properly co-optimizing these factors are the difference between bonding success and failure.



The cost of advanced packaging technology will always be a consideration in the new era of heterogeneous integration. As we integrate more and more chiplets into a single package, designers

want the packages to be larger and larger. As packages grow larger, use of wafers have limitations as only a few large packages can fit into the wafer format. In the future, we need to find a way to port high-density, wafer-level interconnect technologies onto larger substrates.

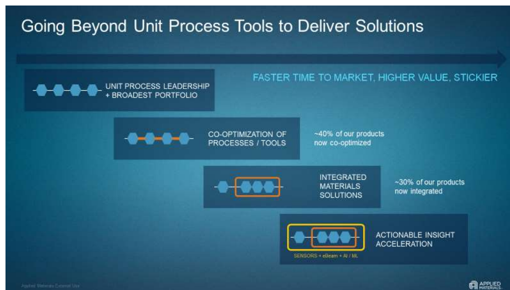
Applied has taken a strategic step in this direction. We recently completed the acquisition of a company called Tango that specializes in PVD deposition on large panels. This enables us to pioneer the market for advanced packaging on 500 millimeter by 500 millimeter panels. The acquisition complements the leadership we already have in PVD technology and also in the display market. Applied also has eBeam inspection technology for the display market, that can be very helpful to our customers pursuing advanced packaging on large substrates.

Another key asset for our customers is Applied's Advanced Packaging Development Center in Singapore, where we have all of the tools and technologies our customers need to develop the world's most advanced packaging technologies, including hybrid bonding. The lab gives us a unique ability to co-optimize process technologies and fully validate their robustness with test vehicles. We have recently introduced to the lab advanced software modeling capabilities to help create co-optimized solutions even more effectively.

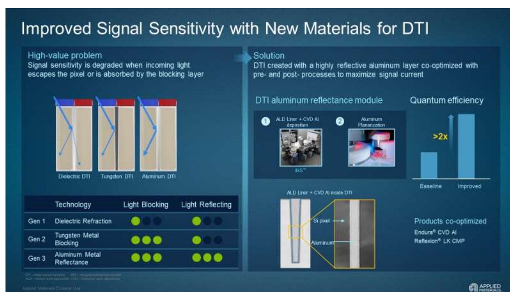
To summarize, heterogeneous design and advanced packaging are the future of PPACt for semiconductor and systems companies. Applied is helping to accelerate the trend with the help of our unique breadth and depth, along with industry partnerships and the world's most advanced lab where we can collaborate with the industry's leading companies. And now, I would like to hand the meeting back to Sundar to talk about the business.

SUNDAR RAMAMURTHY | Group Vice President, Epitaxy, Packaging & ICAPS

Thank you Nirmalya and Mike. Now I'd like to summarize how ICAPS and packaging are going to help us meet the growth targets we outlined at our investor meeting in April. After listening to Mike and Nirmalya, I hope you can see that we are building and funding a strategy that's designed to deliver growth well beyond the model horizon.

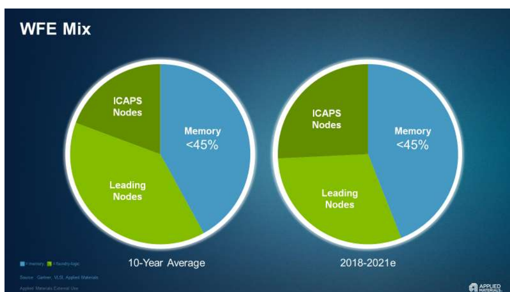


There's a special reason why we formed these solutions businesses within Applied. It's to bring focus to the unique customer needs and the unique technology inflections in these large and growing markets. To innovate solutions better and faster, to accelerate customer R&D and the transfer to high-volume manufacturing. To help do this, we're following the same playbook we use throughout our Semiconductor Products Group businesses. We're using our unique portfolio breadth, co-optimizing across products and steps, and integrating steps when doing so can enable materials and structures that can't be made in any other way.



In ICAPS, for example, Mike talked about CMOS image sensors and how we can use materials engineering to improve photo signals and increase pixel density at the same time by minimizing electrical and optical crosstalk between neighboring photodiodes. Our integrated platform solution is already at customer sites getting qualified for next-generation CIS devices.

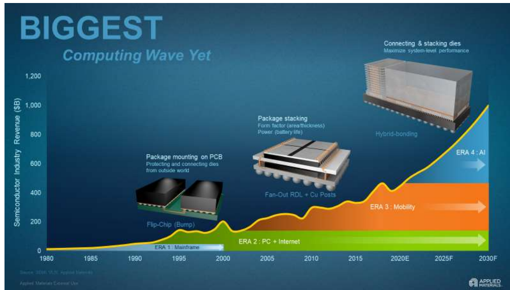
In this market, we are enjoying our close partnership with Sony. The ICAPS organization with its dedicated CIS engineering team allows us to accelerate innovative solutions to address Sony's roadmap challenges by improving CMOS image sensor capabilities in the areas of light sensitivity, resolution and dynamic range. And we've been forming deeper relationships throughout the ICAPS market since we formed the group in 2019. The timing is right for this. As you saw in the introduction today, we referenced 2018 as the start of the fourth wave of computing.



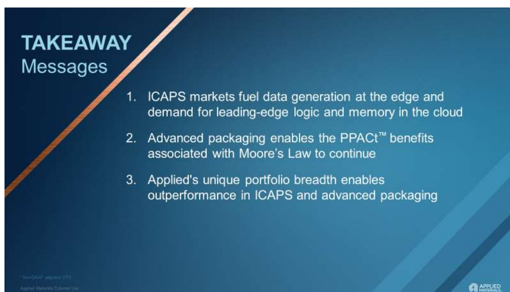
The equipment market has been changing ever since. At the Logic Master Class, we showed you how the equipment market has trended over the past 10 years on average. Memory has been less than 45 percent. Foundry-logic has been more than 55 percent. And within foundry-logic, spending has been about two-thirds on leading nodes and about one-third on ICAPS nodes.

Now let's update the foundry-logic mix to include the fourth wave of computing. Using the four-year average from 2018 through our expectations for 2021, the ICAPS markets have been driving over 45 percent of foundry-logic spending. And in 2020 and our forecast for 2021, spending is balanced between leading edge and ICAPS. In fact, in Applied's fiscal 2021 we now expect over four billion U.S. dollars in ICAPS revenue. We recently announced a large five-year contract with one of the leading ICAPS customers. This gives our customer assured supply and it gives Applied an attractive long-term system and services opportunity.

In packaging, we've shown you our plan to double the business by 2024 from around $500 million in fiscal 2020. This fiscal year we're on track to exceed $800 million, so we're already well on track. But I think the most exciting thing is that we're just getting started.



This year's revenue is backed by our number one positions in bump, bond-pad and TSV. These are the established technologies that are used in PCs and smartphones today. They'll continue to play a role in the AI era, as high-performance computing increasingly moves to heterogeneous design and advanced packaging. But Nirmalya also spoke of hybrid bonding. We expect significant growth beyond our model horizon, both in chip-to-wafer hybrid bonding and in wafer-to-wafer hybrid bonding. In addition, we see the move from silicon wafer substrates to larger advanced substrates. Applied has a broad portfolio to enable this trend. As Nirmalya described, we are working with partners to accelerate the availability of complete solutions for these technologies. And we are already working with all of our major customers to help accelerate their roadmaps.



Now I'll help summarize today's Master Class which is all about powering the fourth wave of computing, which is the biggest inflection in our lifetime. ICAPS and advanced packaging both have a critical role in enabling the future. In fact, they complement one another and create a virtuous cycle for semiconductor growth. ICAPS is about putting intelligence into all things, eventually trillions of things. And while we are at it, electrifying the automotive industry. Heterogeneous design and advanced packaging are about enabling the PPACt, including the most powerful AI chips in the data center. With classic Moore's Law slowing, advanced packaging is the future of PPACt. And finally, Applied's unique portfolio breadth will allow us to drive these markets and outperform.

On a personal note. I've been at Applied for over 25 years, including as General Manager of leadership businesses, such as PVD and epi. I'm used to seeing Applied enable our customers' roadmaps. I'm honored to be leading the ICAPS and advanced packaging businesses at Applied, and I'm more excited than ever about the role we're playing in the industry. So, thank you for your time today. And now Mike, let's start the Q&A.