New Ways to Wire and Integrate Chips

MASTER CLASS
May 26, 2022

Forward-Looking Statements and Other Information

Today's presentations contain forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our investment and growth strategies, our development of new products and technologies, forecasts relating to our revenues, market share and other financial and business performance, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; transportation interruptions and logistics constraints; global economic, political and industry conditions, including rising inflation and interest rates; the effects of regional or global health epidemics, including the severity and duration of the ongoing COVID-19 pandemic and government imposed lockdowns and other measures taken in response; global trade issues and changes in trade and export license policies; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; acquisitions, investments and divestitures; changes in income tax laws; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

Applied Materials, the Applied Materials Logo, and other trademarks so designated as product names are trademarks of Applied Materials, Inc. Other names and brands are the property of third parties.

2022 MASTER CLASSES

WELCOME

Michael Sullivan

Corporate Vice President

Head of Investor Relations

NEW WAYS TO WIRE AND INTEGRATE CHIPS MASTER CLASS | MAY 26, 2022

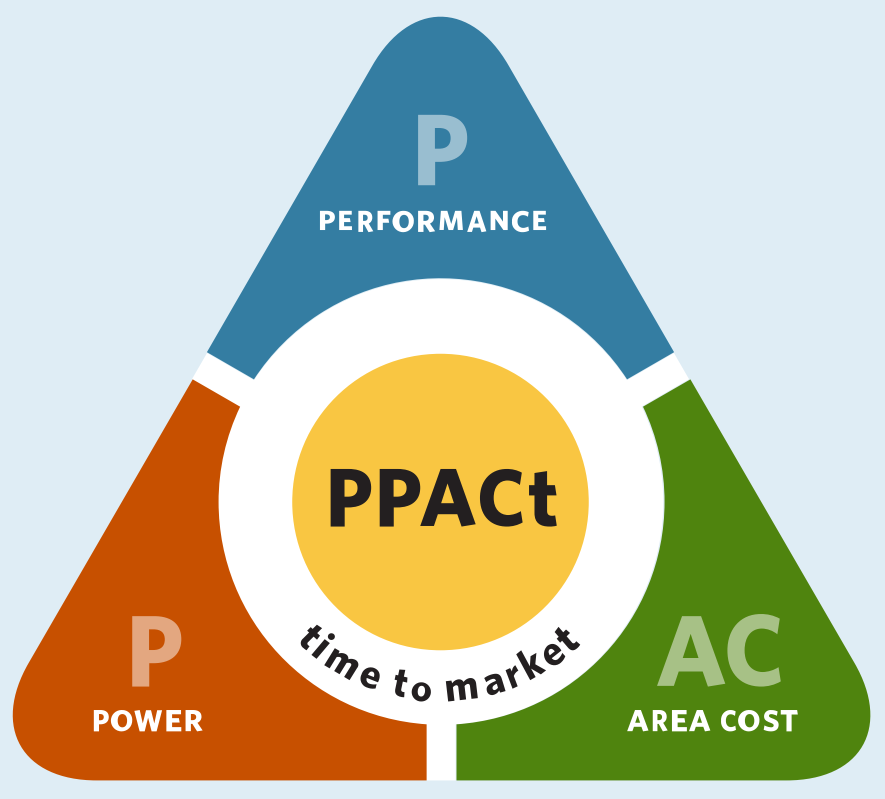
2022 Master Classes

APRIL 21

New Ways to Shrink

MAY 26

New Ways to Wire and Integrate Chips

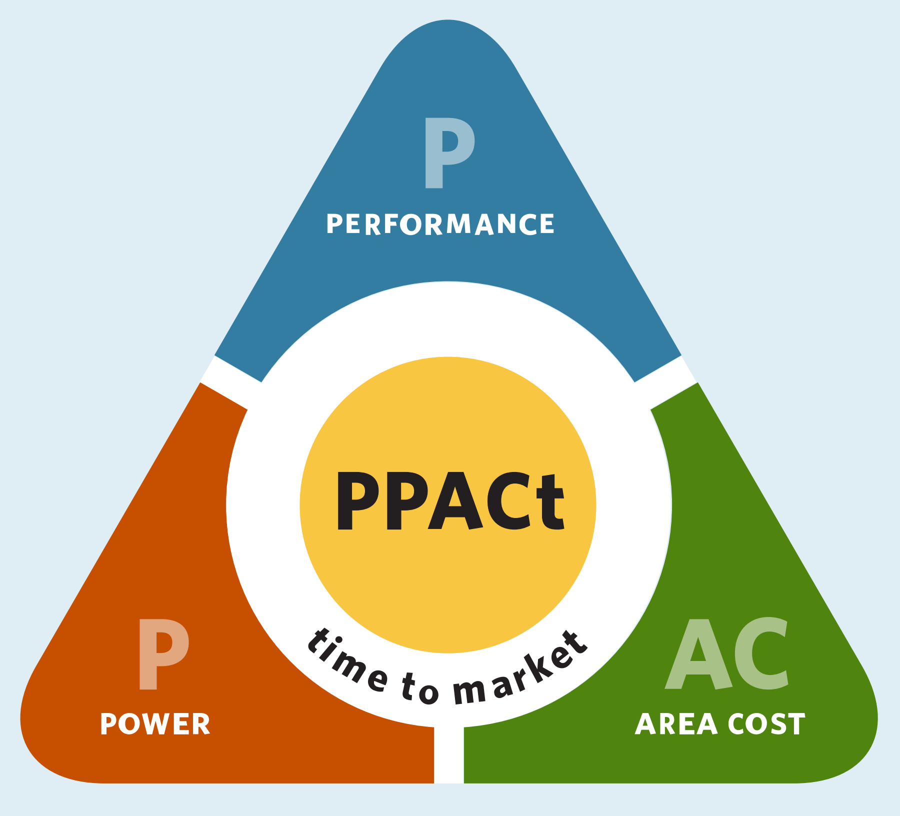


AGENDA

9:00	PART 1	**Mike Sullivan** Introduction and Fireside Chat with Regina Freed
9:05	PART 2	**Kevin Moraes, Ph.D.** Solving the Resistance Challenges of EUV Scaling **Mehul Naik, Ph.D.** Enabling Backside Power Distribution Networks **Sundar Ramamurthy, Ph.D.** Enabling Heterogenous Chip Integration with Hybrid Bonding and Advance Substrates
9:45	PART 3	**Raman Achutharaman, Ph.D.** Growth in Chip Wiring and Integration
9:50	PART 4	**Q&A** Mehul, Sundar, Raman, Mike

2022 Master Classes

APRIL 21	MAY 26	Sept 22*
New Ways to Shrink	New Ways to Wire and Integrate Chips	Subscriptions and Services



* Target date

FIRESIDE CHAT

Regina Freed
Vice President
Semiconductor Products Group

APPLIED MATERIALS

Solving the Resistance Challenges of EUV Scaling

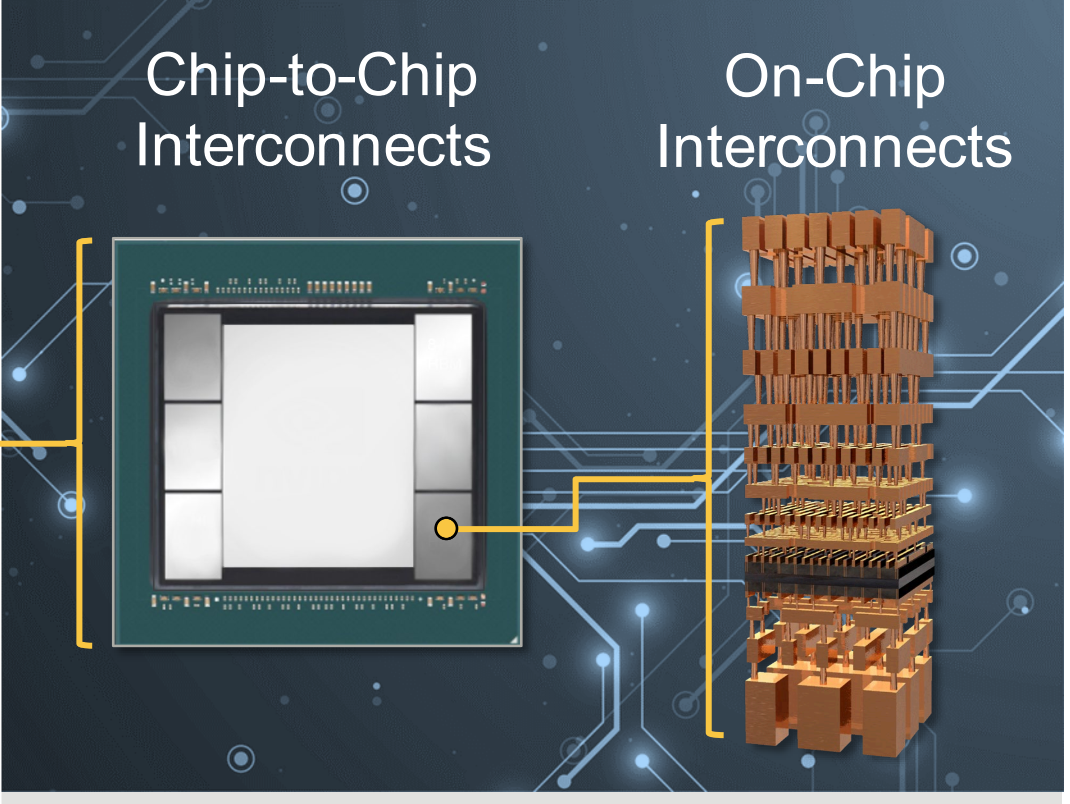
Kevin Moraes, Ph.D.

Vice President

Semiconductor Products Group

NEW WAYS TO WIRE AND INTEGRATE CHIPS MASTER CLASS | May 26, 2022

Creating Amazing Digital Experiences with Billions of Transistors



Brought to you by:

1. Low-resistance wiring
2. Backside power distribution networks
3. Heterogenous integration

Wiring Transistors On a Chip

Interconnects

Lines + Vias

- Make connections laterally and vertically
- Over 15 metal layers
- 4-5 layers at minimum pitch
- Smallest widths ~14nm

Contacts

Via contacts
Trench contacts
Gate
Fin

- Connect transistors to interconnects
- One or two metal layers
- Smallest widths ~12nm

Image source: TechInsights and Applied Materials

Creating Transistor Contacts

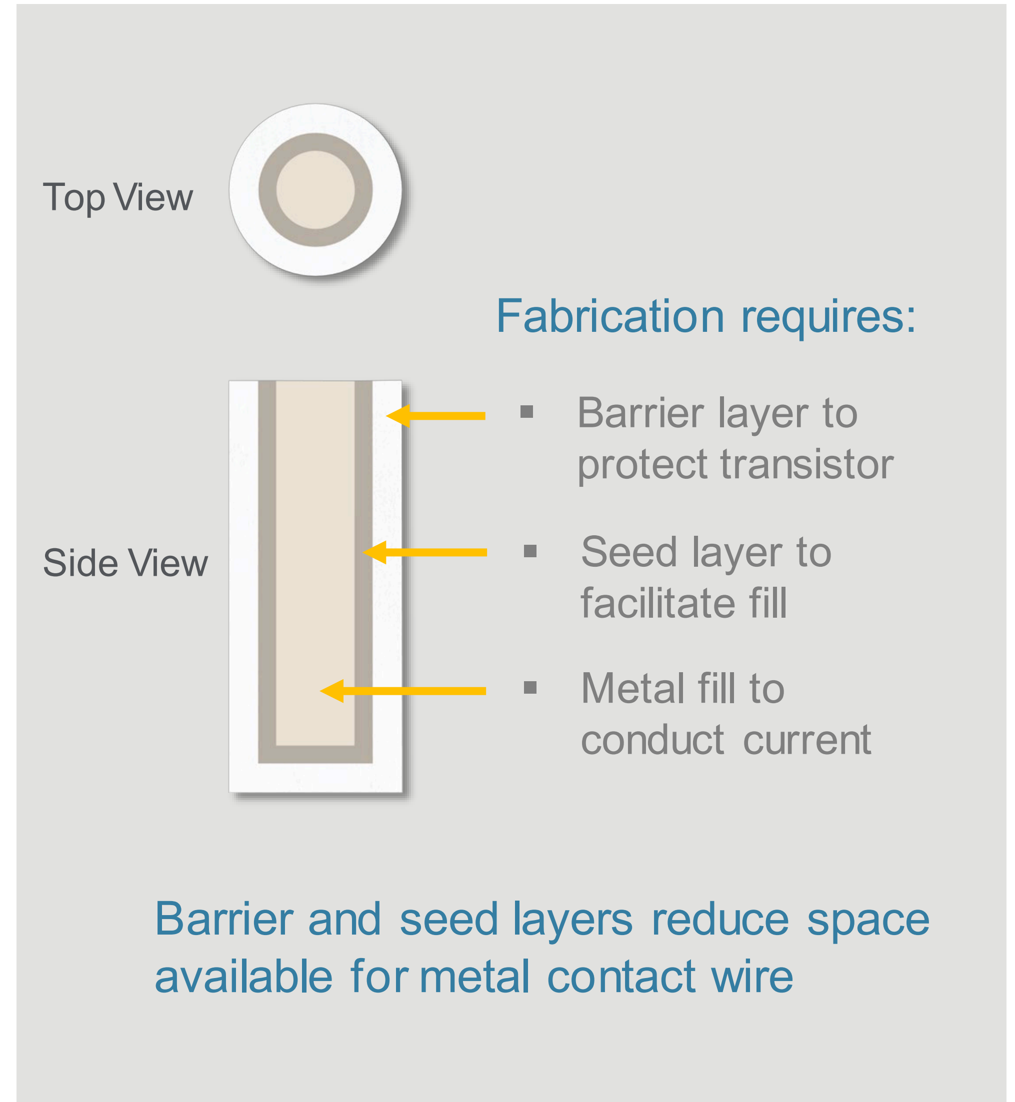
Via contacts

- Connect contact to interconnect
- Bottleneck for current flow

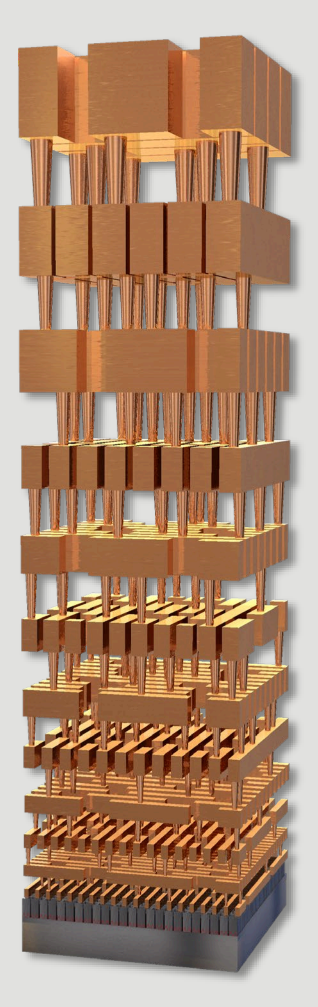
Trench contacts

- Connect contact to transistor
- Must not contaminate channel

Contacts made of tungsten or cobalt



Creating Interconnects Between Transistors

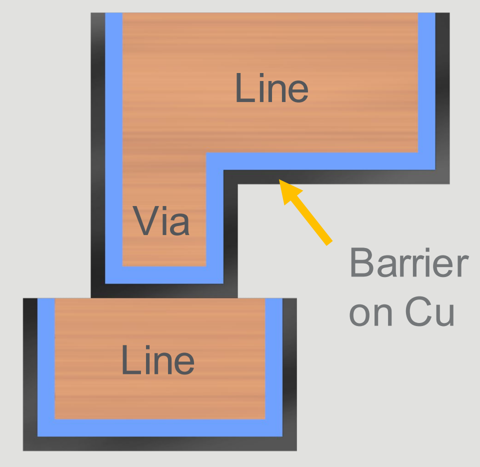


Interconnects

- Lines make lateral connections within each layer; vias connect layers

Chips have >50 miles of copper interconnect wiring

Resistance impacts power and performance



Fabrication requires:

- Barrier to block copper diffusion
- Liner to improve copper adhesion
- Seed layer for copper growth
- Copper fill to complete wire

Barrier layers increase via resistance, cause RC delays, waste power

Resistance Increases Exponentially as Wiring Scales

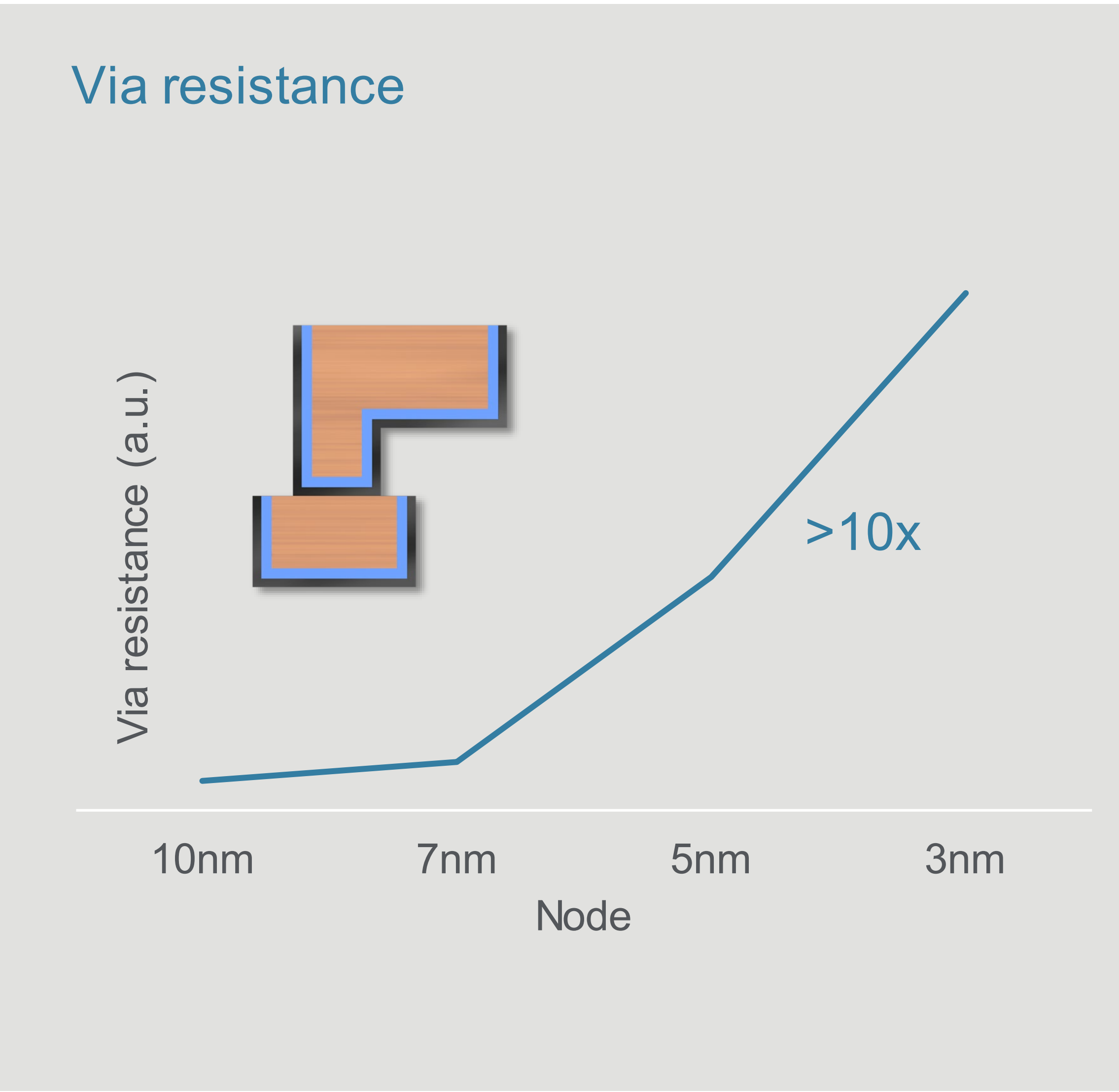
Contact resistance

Contact resistance (a.u.)

>4x

10nm 7nm 5nm 3nm

Node

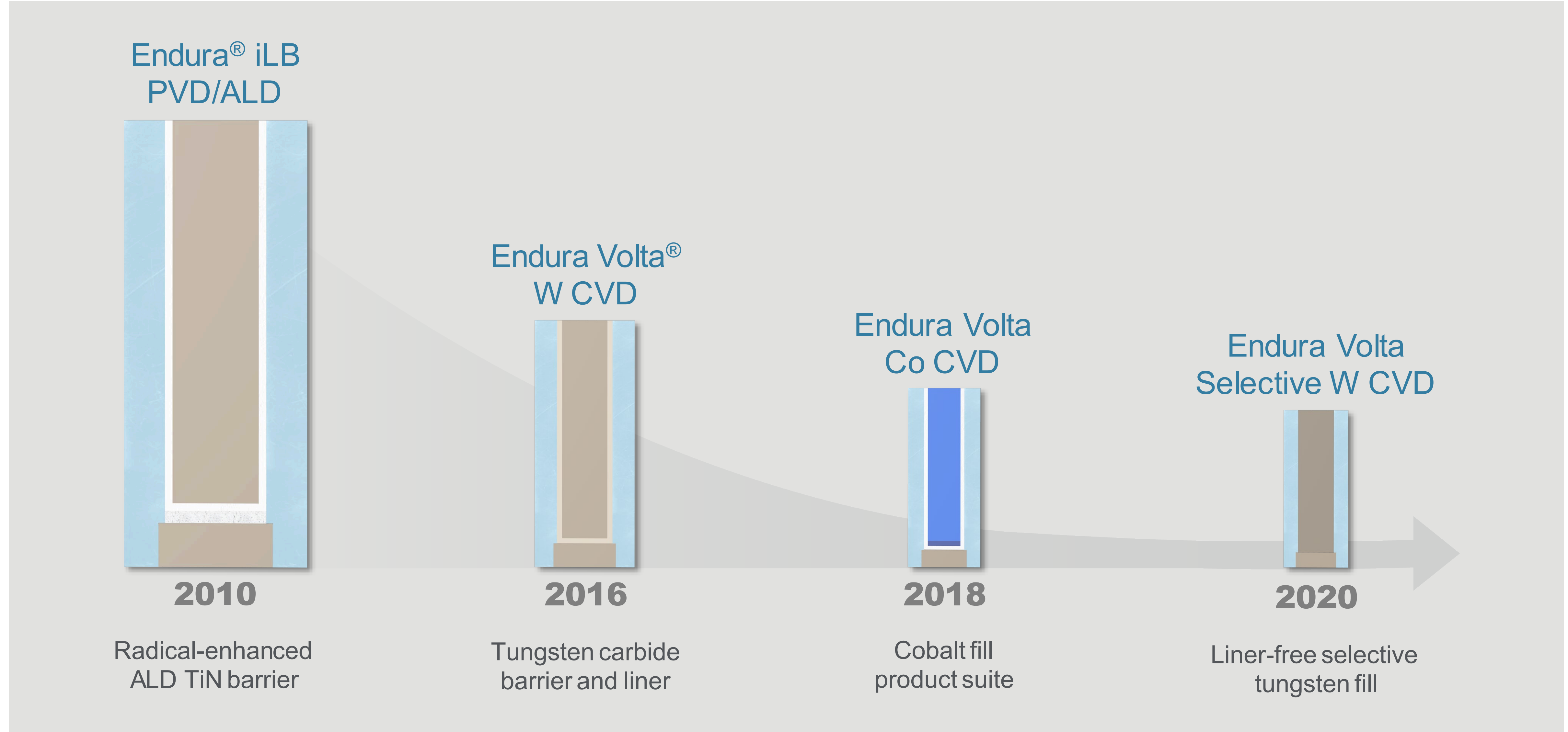


Assumptions: Dimensions scale; liner/barrier materials and dimensions do not

a.u.: arbitrary units

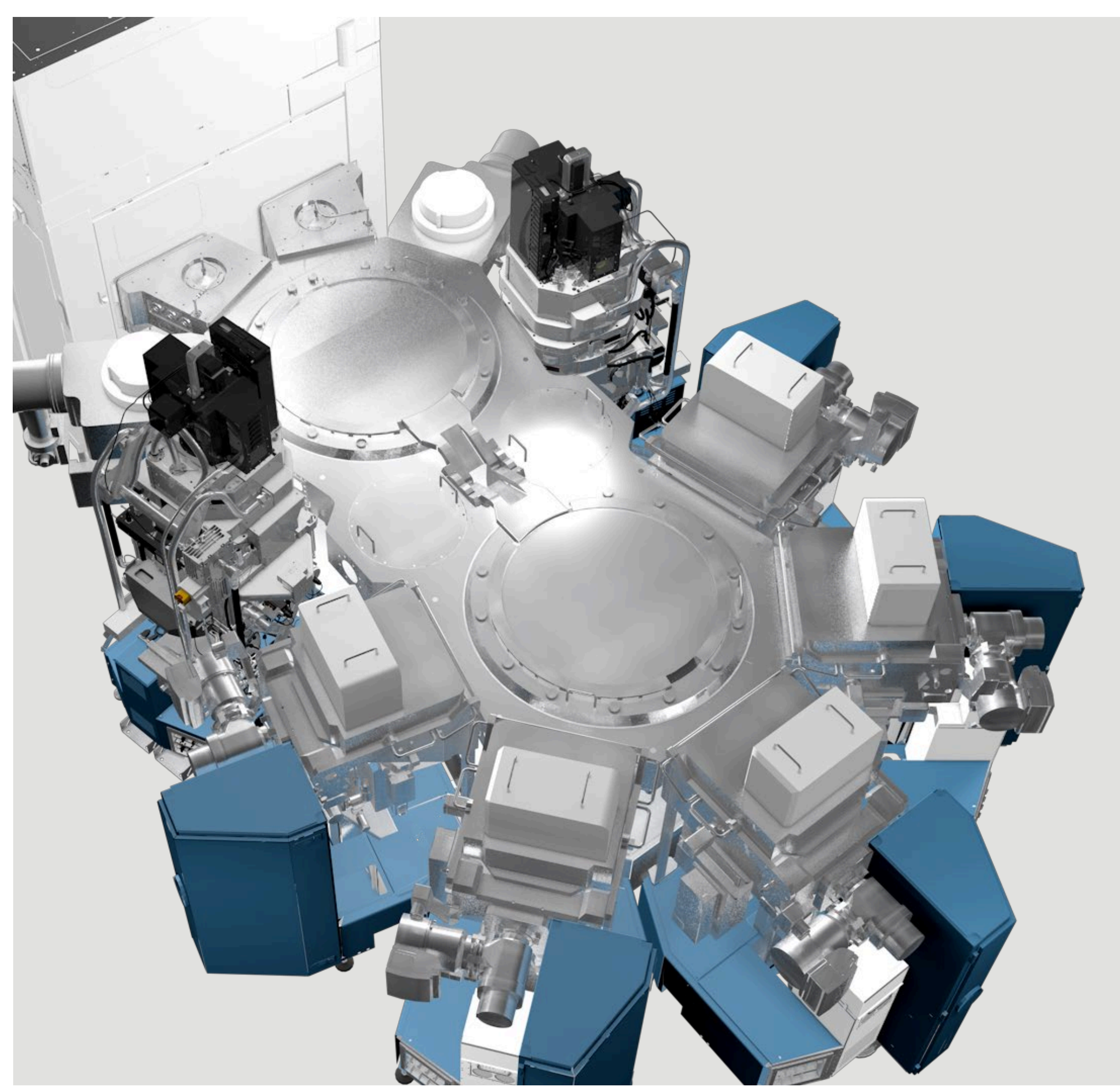
APPLIED MATERIALS®

Contact Resistance Innovations



APPLIED MATERIALS®

Endura Ioniq™ W PVD: Low-Resistance Tungsten Contacts



Integrated Materials Solution™ for pure tungsten metal gapfill

- Combines interface engineering, PVD and CVD in high-vacuum
- Enables contact scaling in a wide variety of applications

APPLIED MATERIALS®

Endura Contact Metal IMS™ System

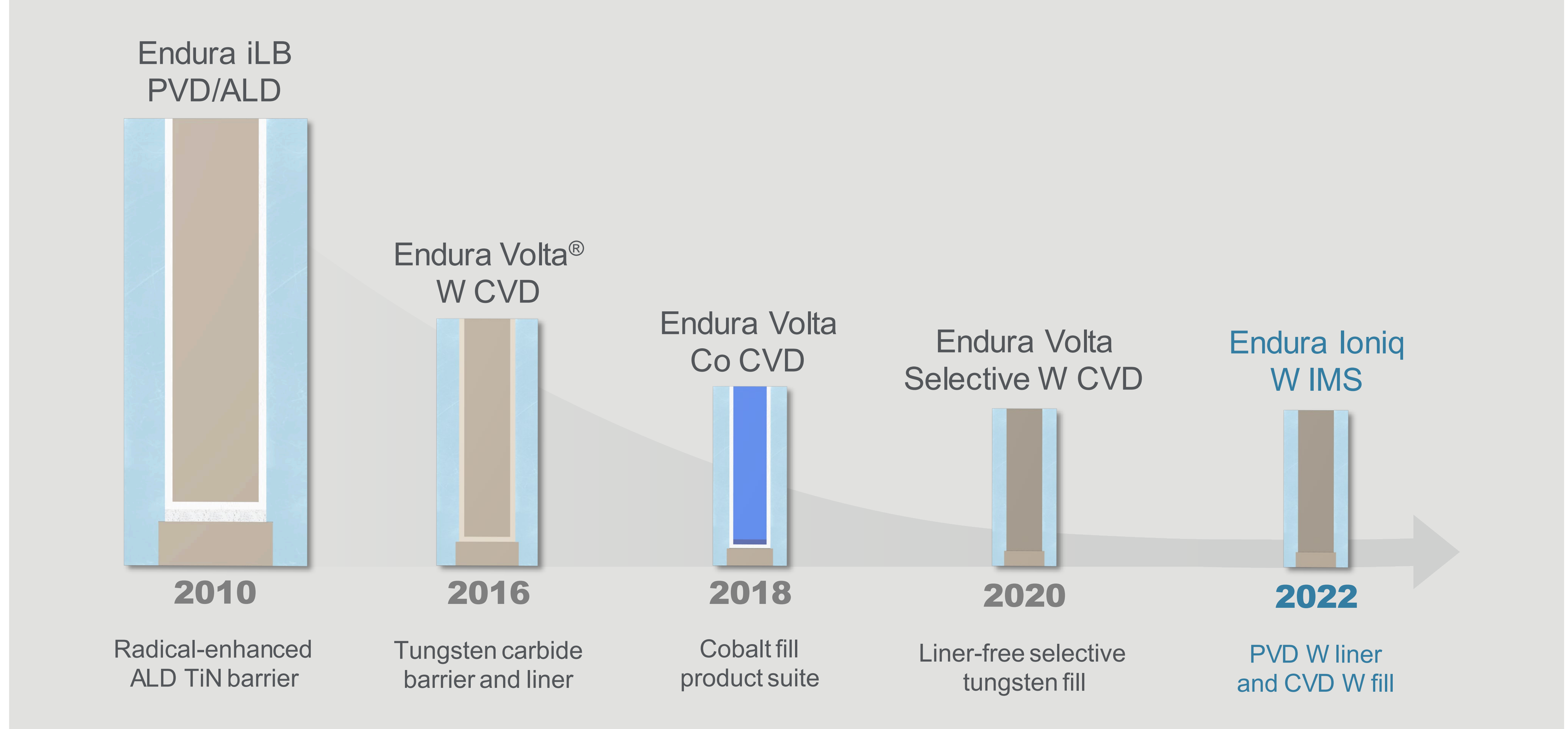
Pure W fill

Pure W liner

Metal surface treatment

Integrated Materials Solution Enables Pure Metal Contacts

Contact Resistance Innovations Continue



Innovations to Extend Copper Interconnects

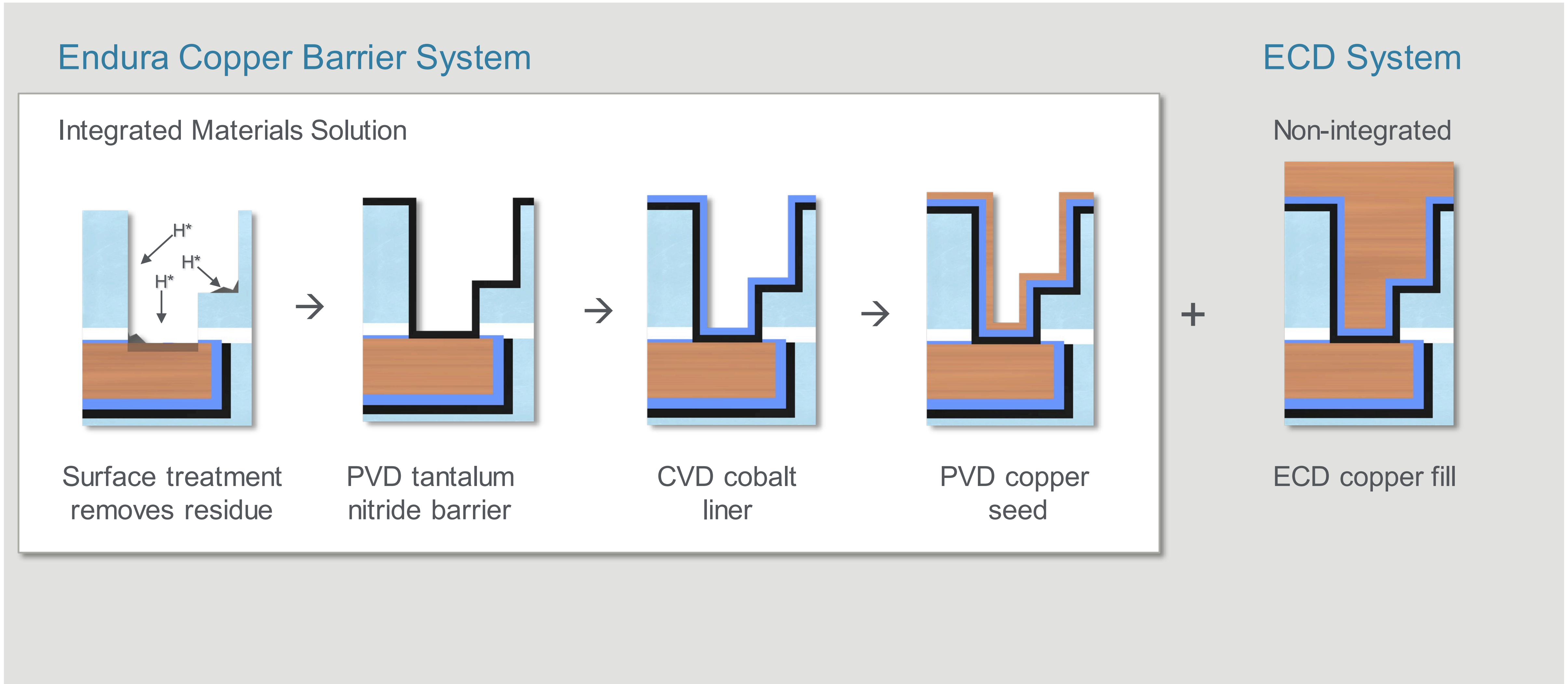
2012
Endura CuBS RF XT PVD
High-coverage barrier & seed

2014
Endura Volta Cobalt CVD
Seed enhancing cobalt liner & selective metal cap

2018
Endura CuBS ALD/PVD
ALD barrier

2021
Endura Copper Barrier Seed IMS
Selective barrier & copper reflow

Copper Interconnect Fabrication



APPLIED MATERIALS®

Challenges Extending Copper Interconnects at 5nm

Exponential resistance increase

Via resistance (a.u.)

10nm 7nm 5nm 3nm

Node

1 Limited space for metal wire

2 High-resistance interfaces

Gapfill limitations of ECD

>20nm Top Opening

PVD Cu seed ECD bottom-up Cu fill

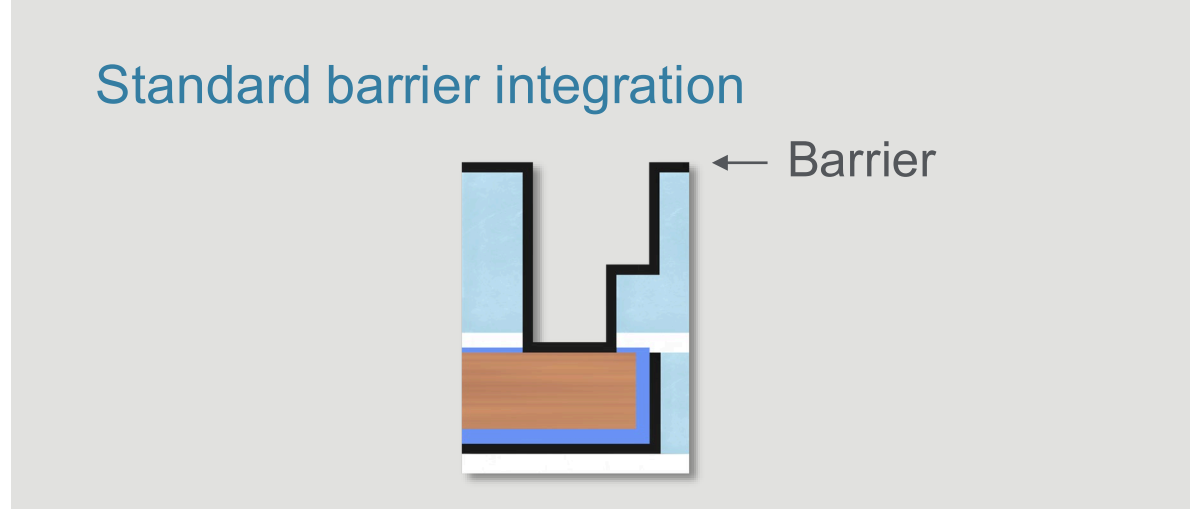
<20nm Top Opening

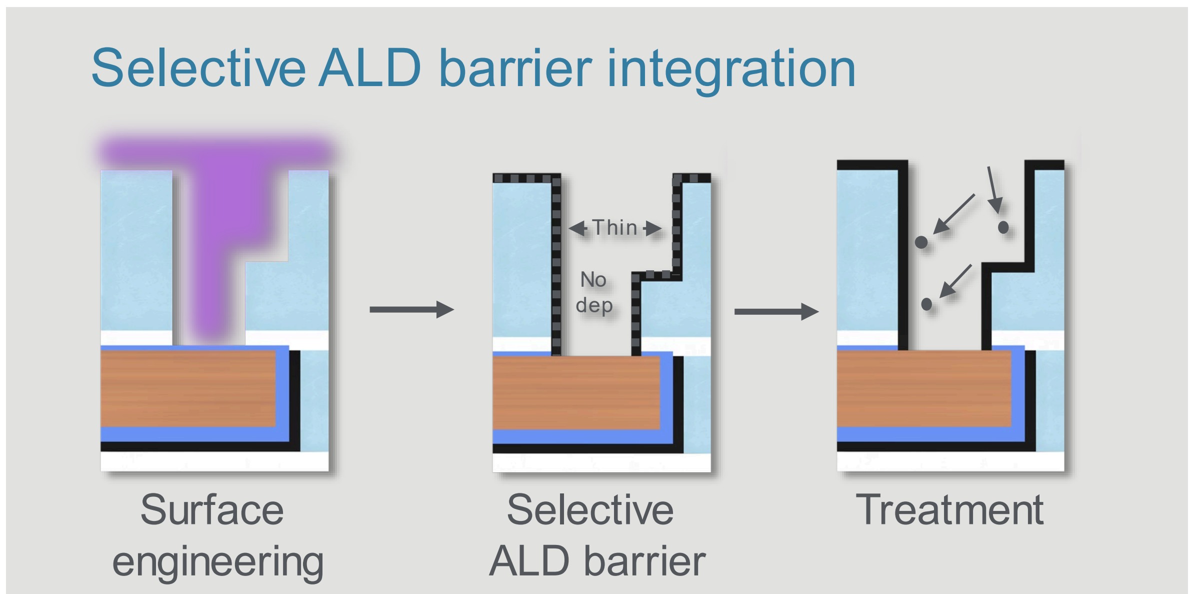
PVD Cu seed ECD bottom-up Cu fill

3 Trapped voids

a.u.: arbitrary units

Lowering Via Resistance with Selective ALD Barriers





Via resistance reduction

Standard Barrier

+100%

-47%

+5%

Selective ALD barrier

Via resistance (a.u.)

5nm

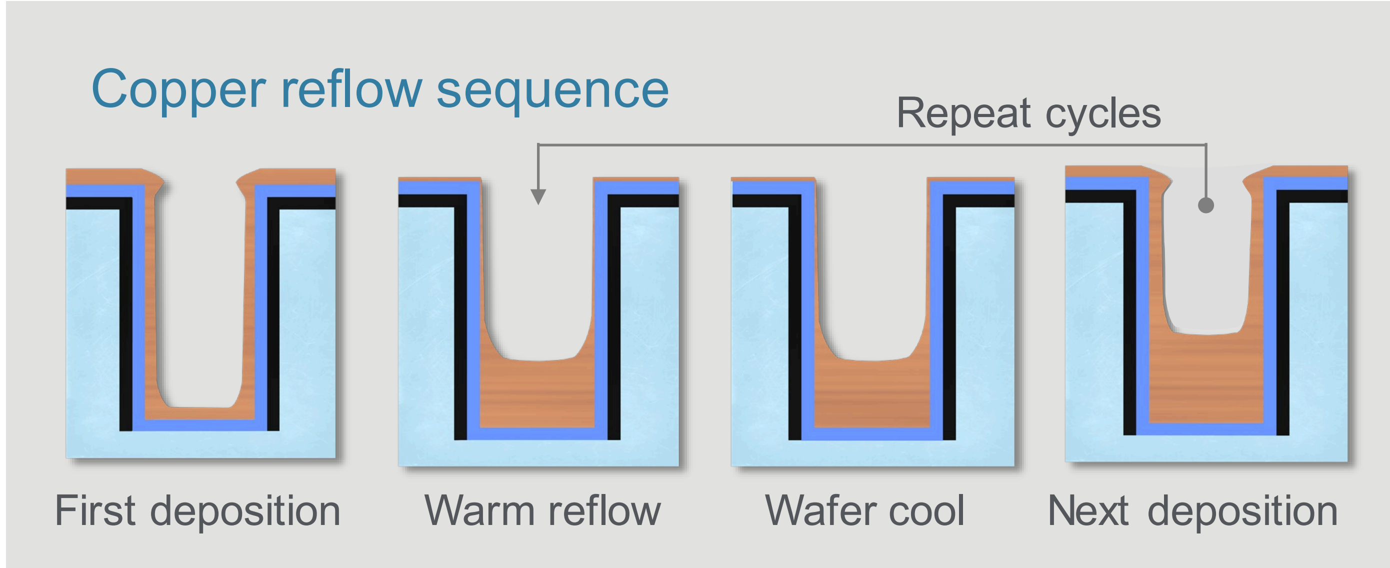
3nm

Node

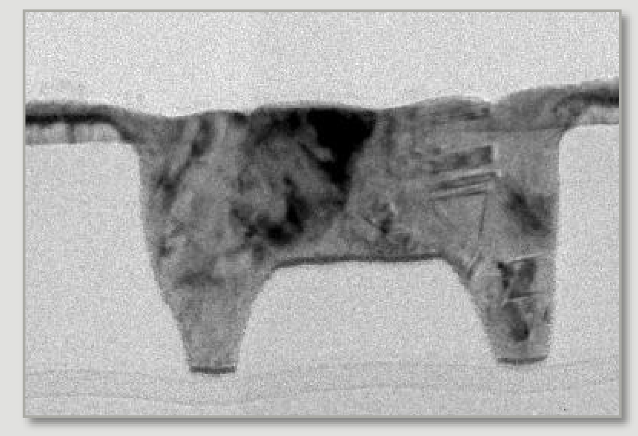
Selective ALD removes high-resistance interface

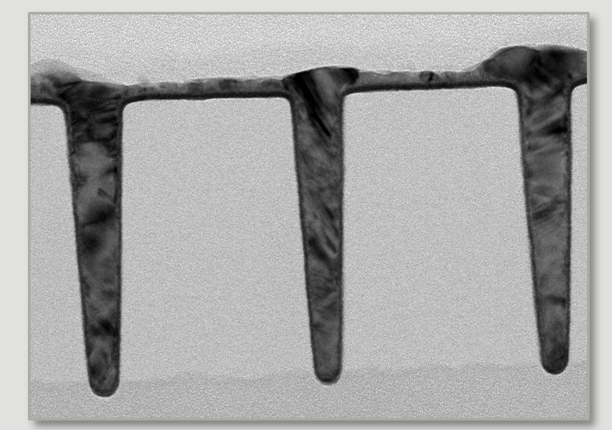
APPLIED MATERIALS

Reliable Copper Gapfill with PVD Copper Reflow



Complete fill with PVD copper reflow





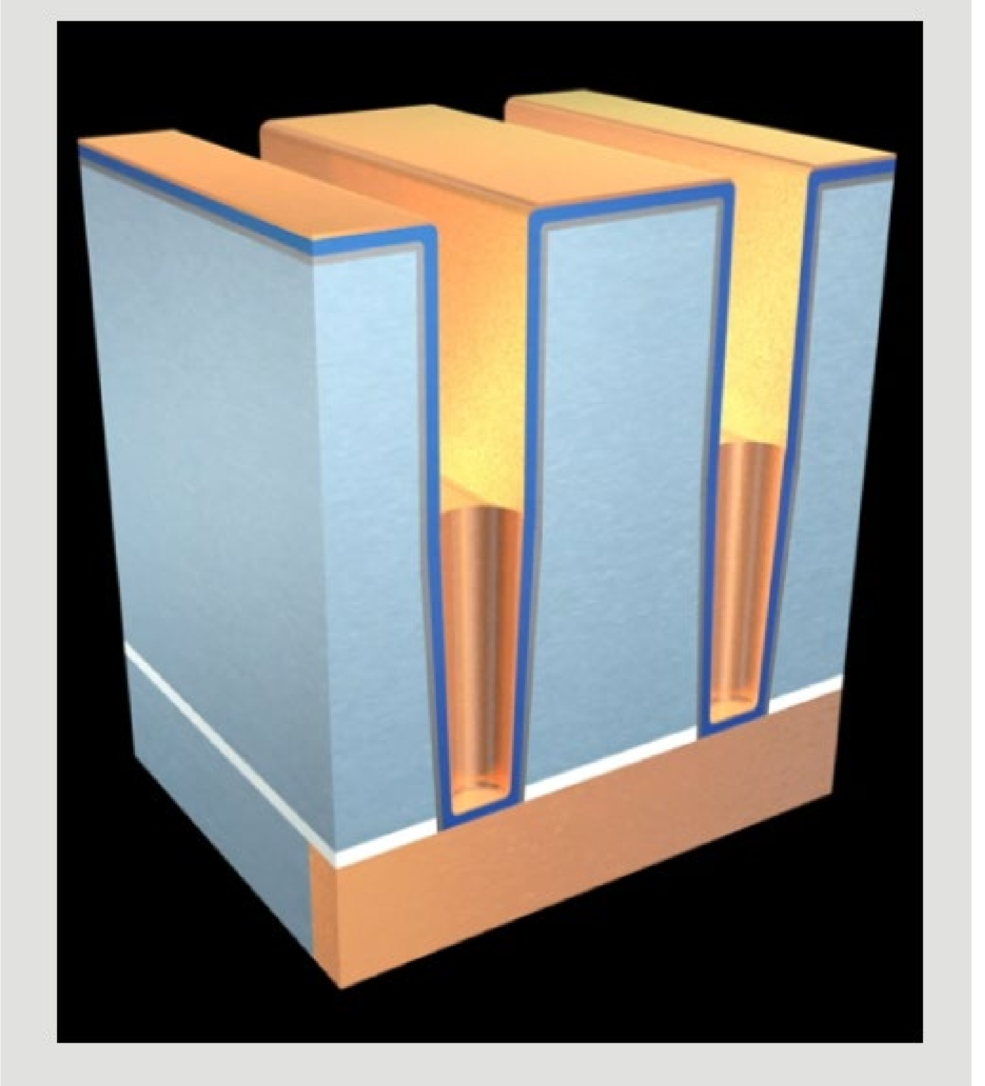
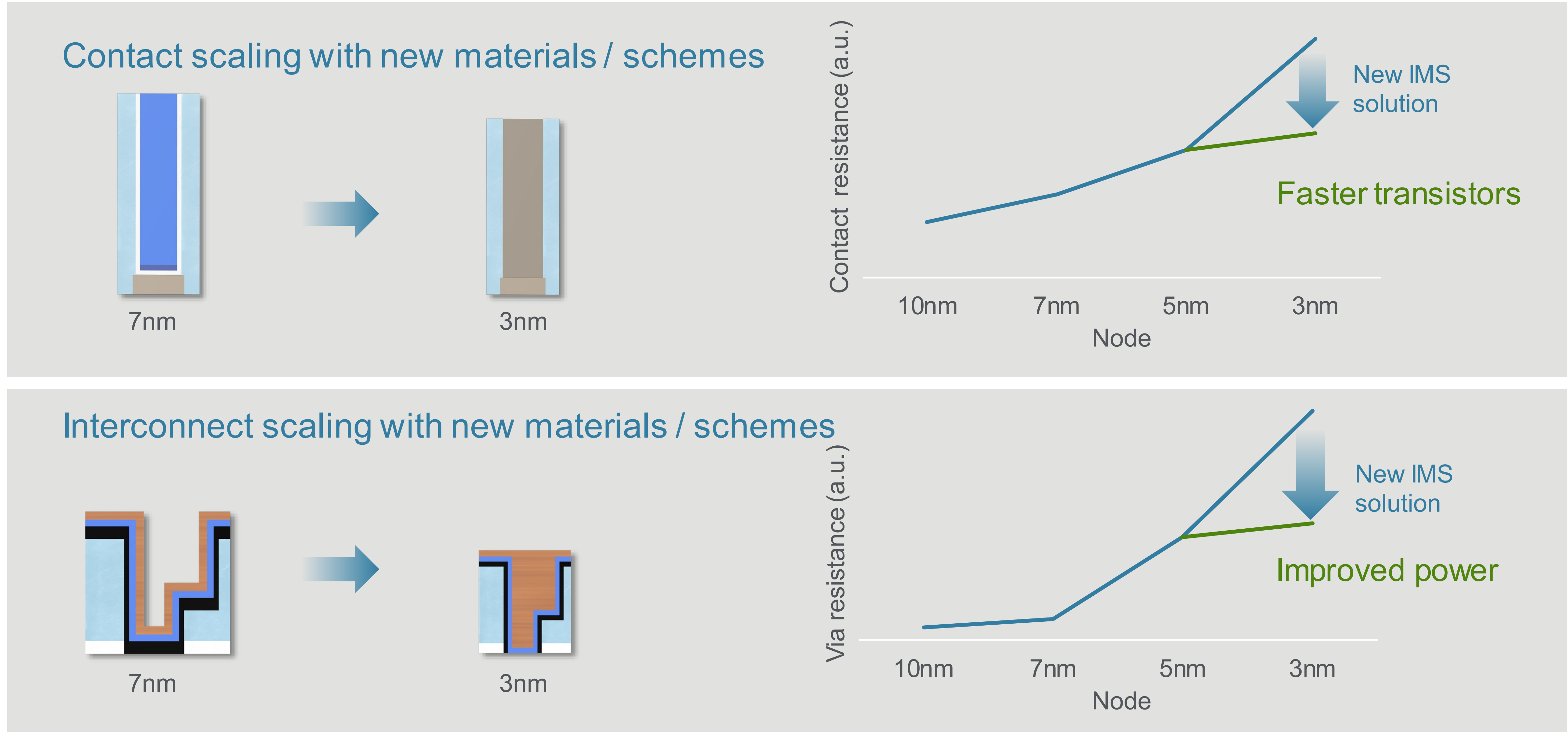


Image source: Applied Materials

Applied Materials External

Unique IMS Solutions Address Resistance Issues of EUV Scaling



APPLIED MATERIALS

Enabling Backside Power Distribution Networks

Mehul Naik, Ph.D.

Managing Director and Principal Member of Technical Staff

Semiconductor Products Group

NEW WAYS TO WIRE AND INTEGRATE CHIPS MASTER CLASS | May 26, 2022

Device Scaling Approaches

Intrinsic Scaling

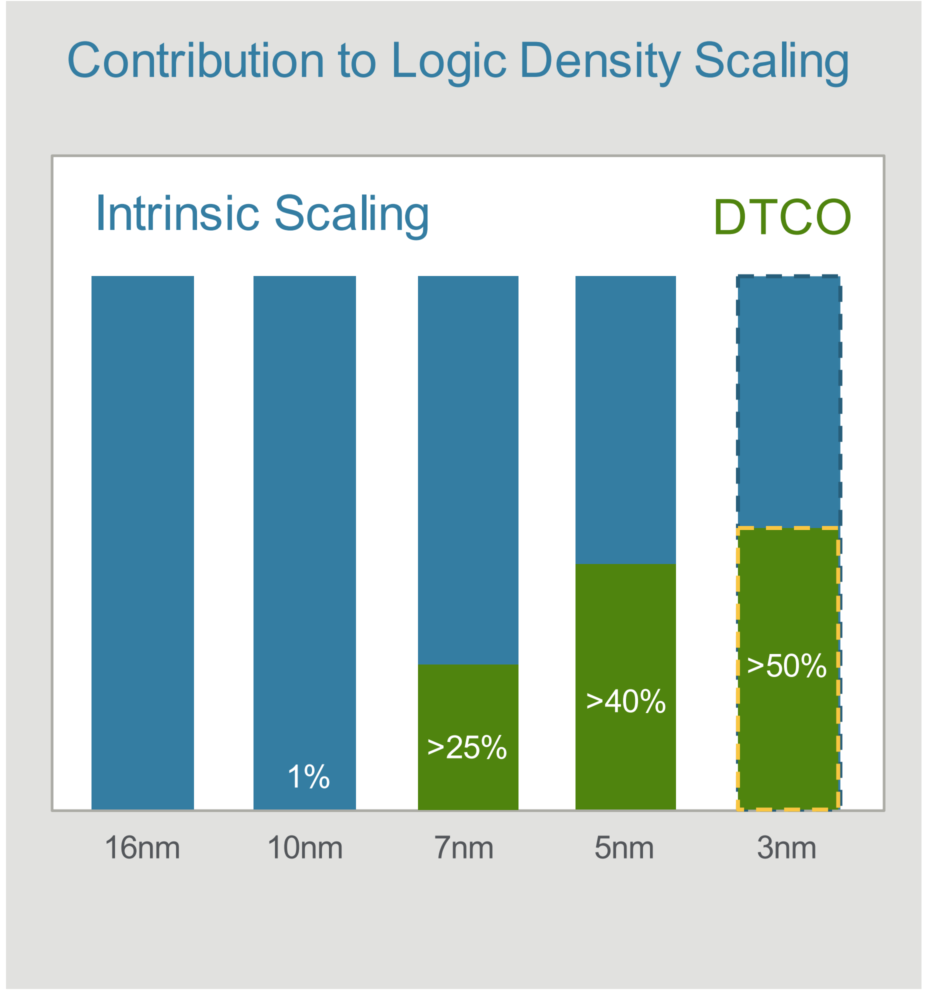
DTCO

N

N+1

N

N+1

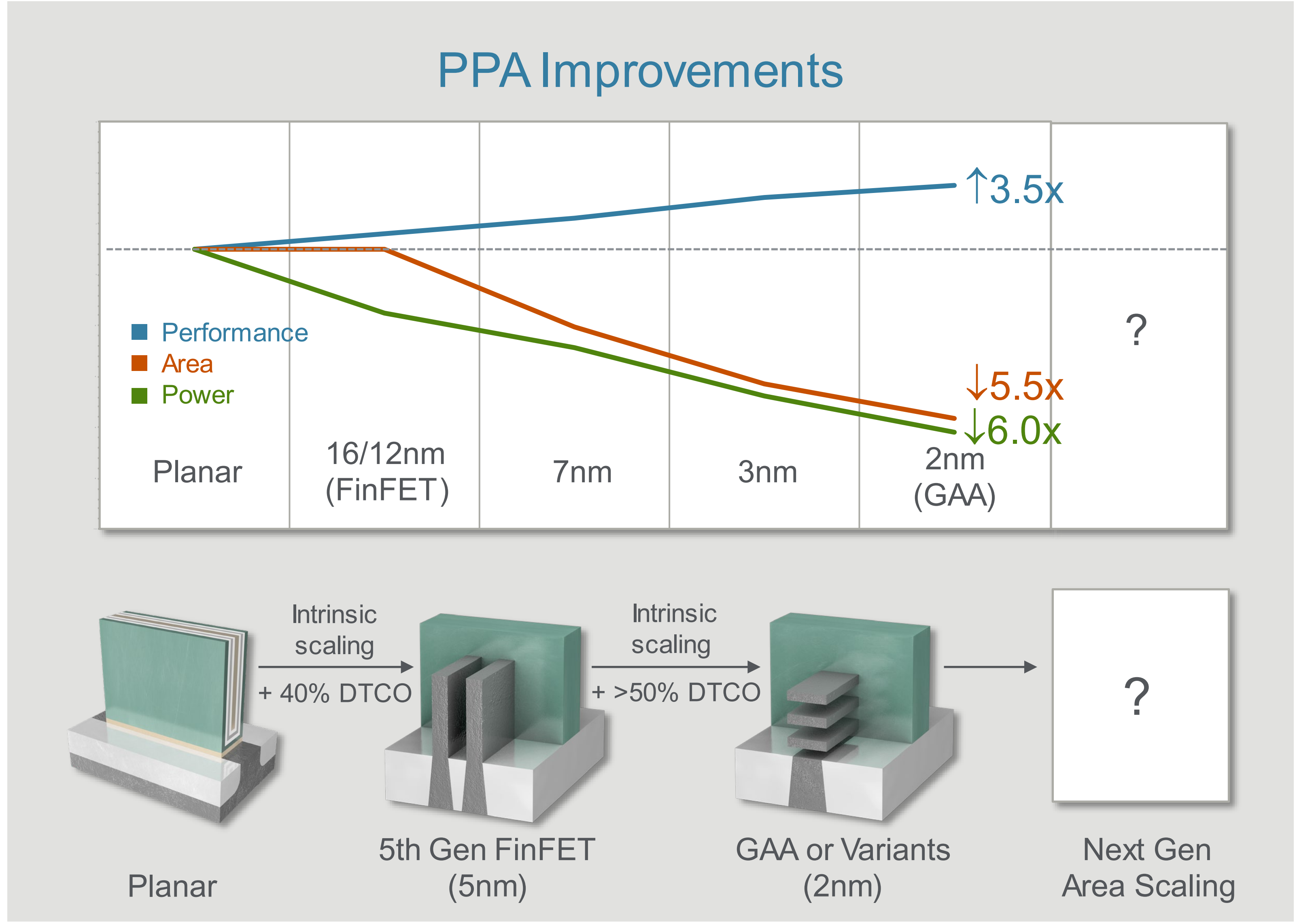


Source: M. Liu/TSMC, ISSCC 2021

DTCO: Design Technology Co-Optimization

DTCO is becoming an increasingly important contributor to scaling

Future of Logic Scaling

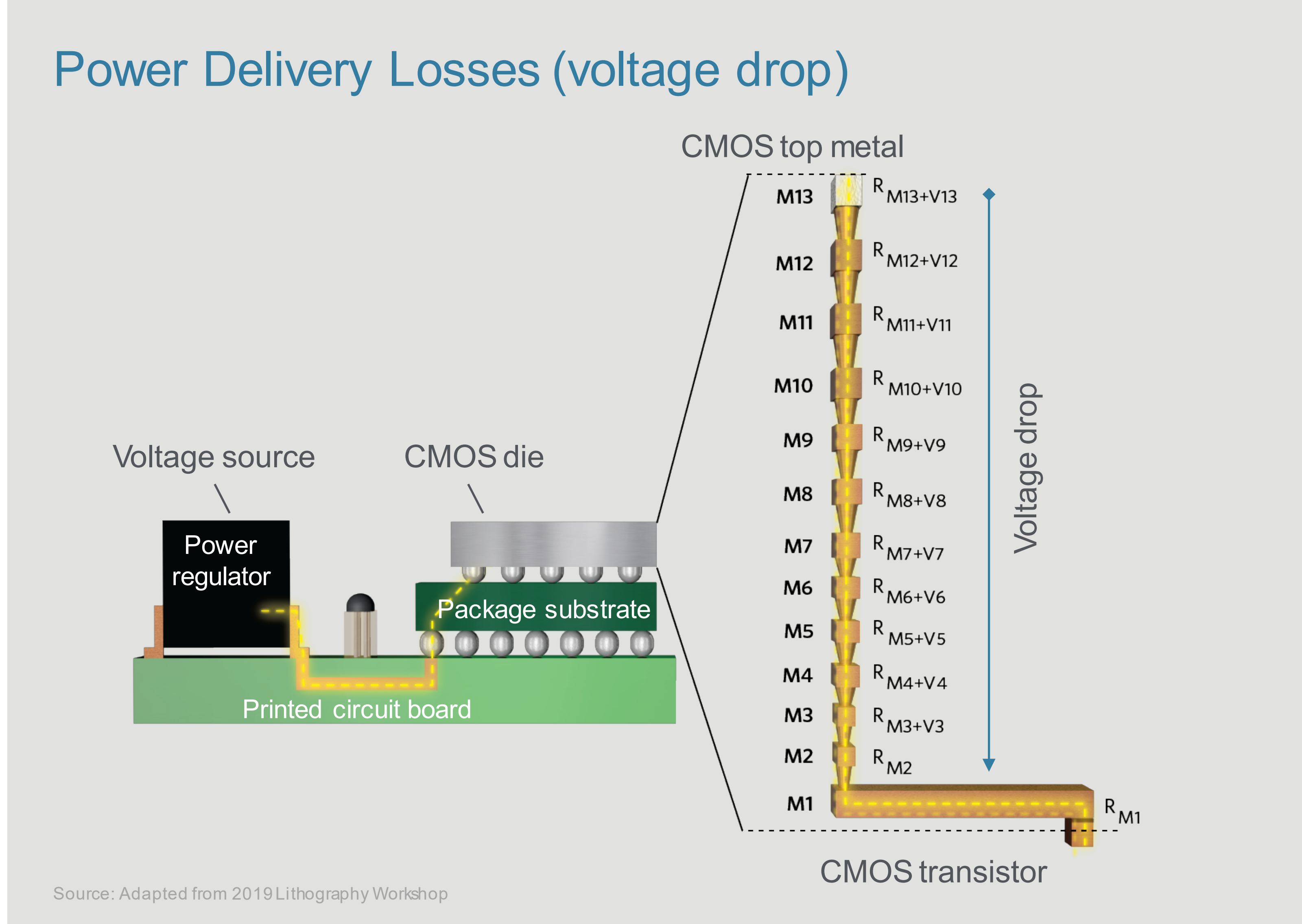


Scaling Benefits

Performance	3.5x ↑
Power	6.0x ↓
Area	5.5x ↓

APPLIED MATERIALS®

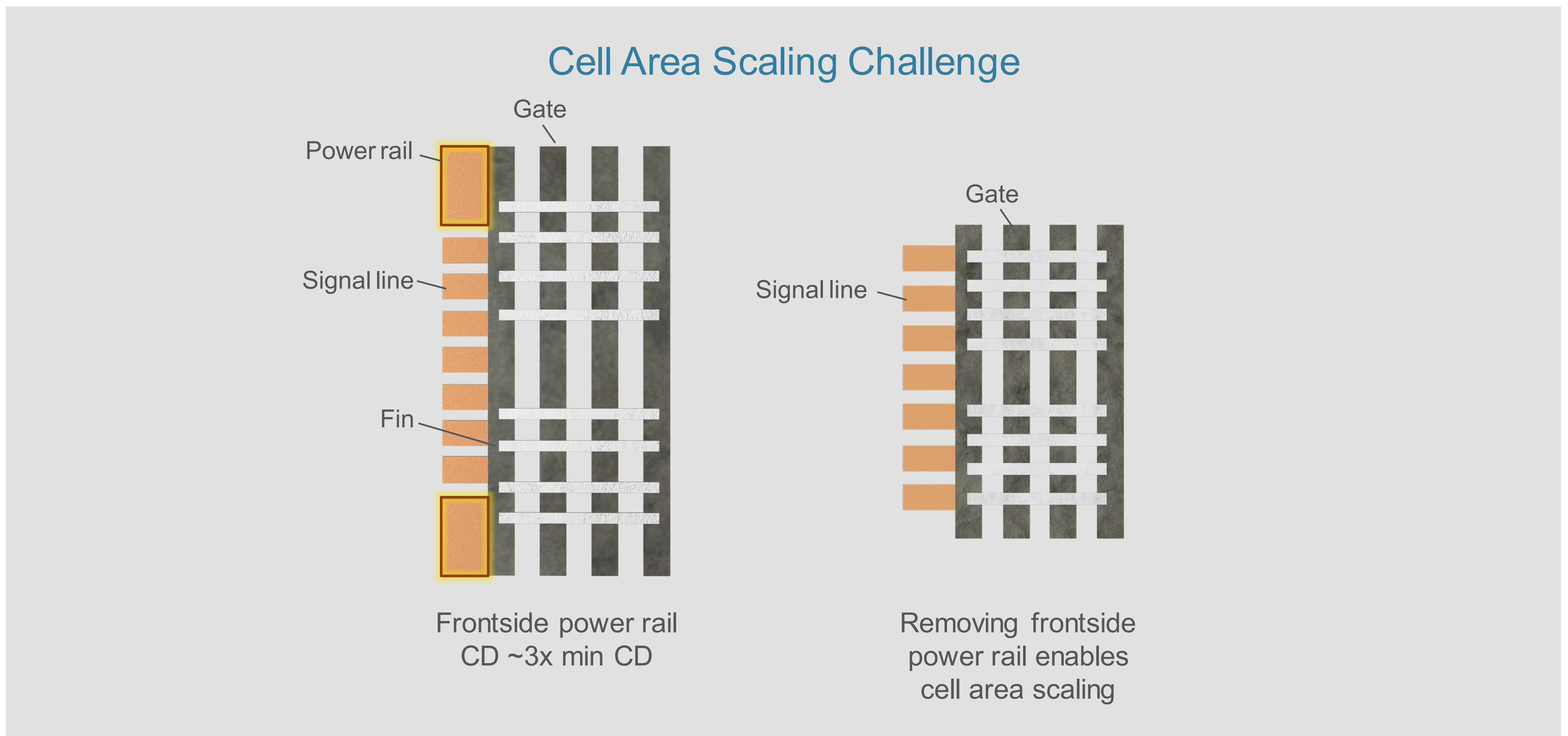
Limitations of Frontside Power Distribution Network Architecture



- Power delivery network design margin permits 10% IR drop
- Large IR drop from 12+ metal levels due to resistance
- Excessive IR drop (~50%) creates reliability issues

APPLIED MATERIALS®

Limitations of Frontside Power Distribution Network Architecture



APPLIED MATERIALS

PPACt Benefit of Backside Power Distribution Network Inflection

Frontside Scheme

Backside Scheme

Power delivery

Power and signal lines

Power rail

Transistor

Signal lines only

Power rail

Power line

Power delivery

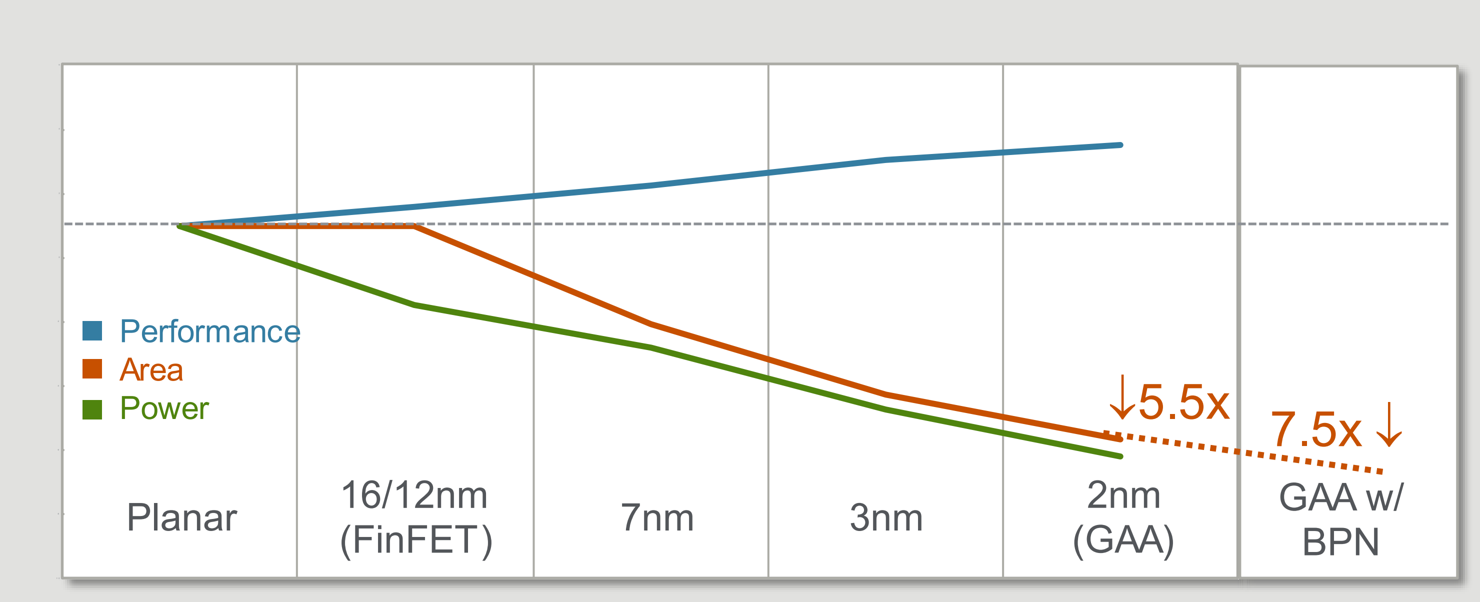
Key changes

- Separation of power and signal lines
- Power delivery from backside of the wafer

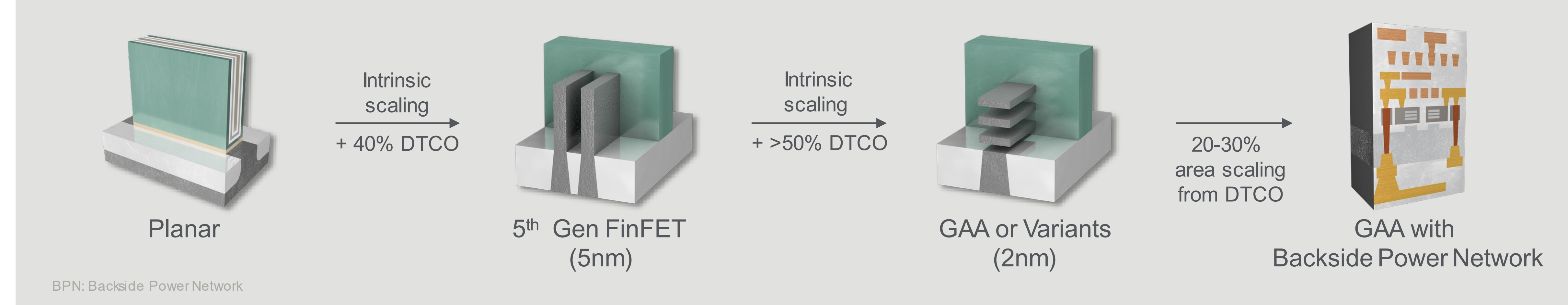
Source: Adapted from multiple IMEC and ARM publications

Reduced Voltage Drop	Maintain 10% design margin
Area Savings	20 to 30% cell area reduction

GAA with Backside Power Network for Additional Area Scaling



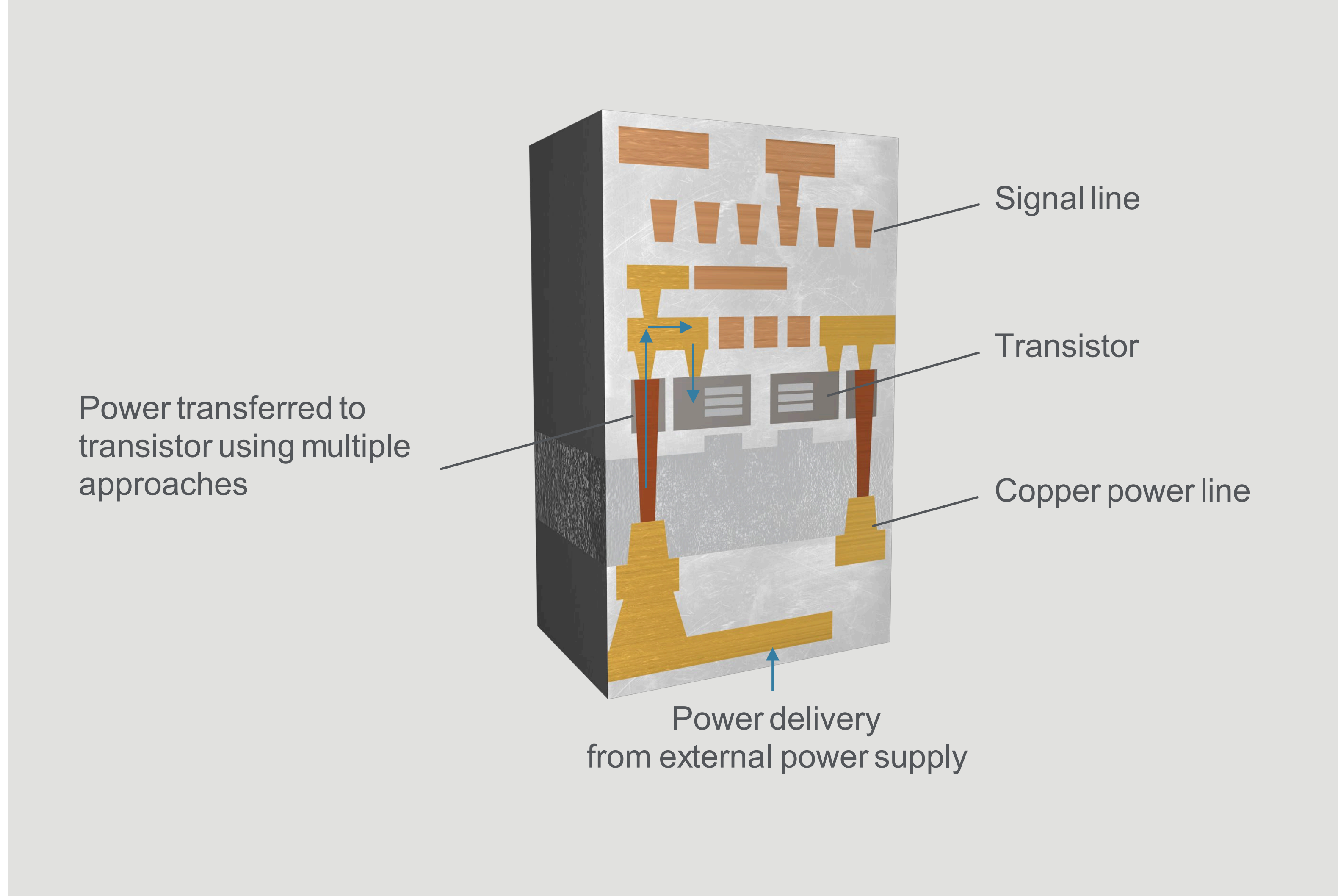
20 to 30% cell area reduction with Backside Power Network



BPN: Backside Power Network

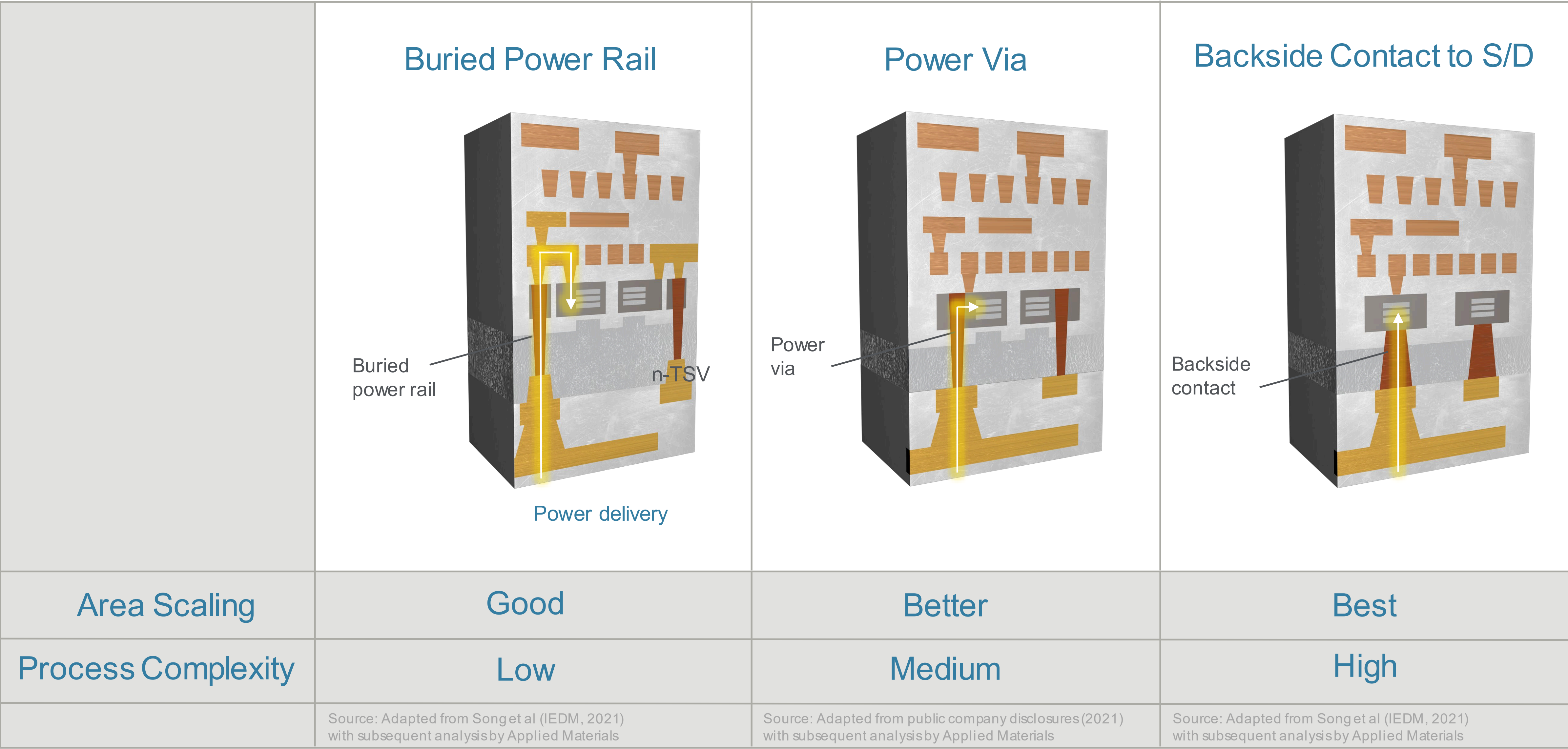
APPLIED MATERIALS®

Backside Power Distribution Network Architecture



- Multiple approaches in development
- Trade-offs between power/area scaling and manufacturing complexity

Announced Backside Power Distribution Network Approaches

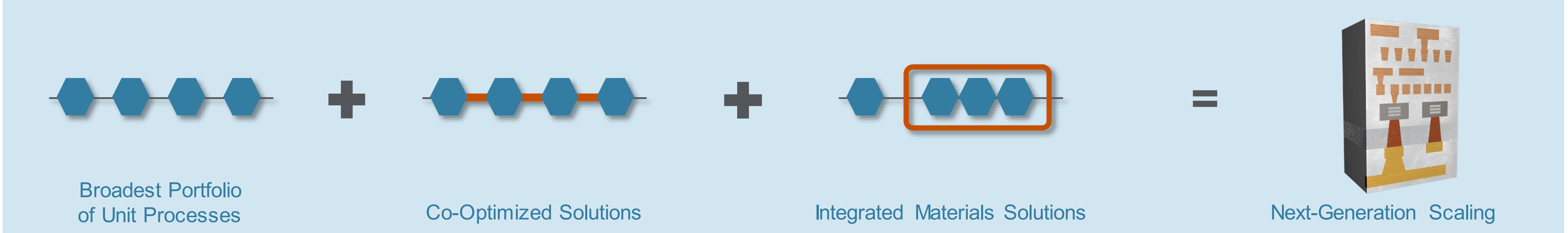


	Buried Power Rail	Power Via	Backside Contact to S/D
Area Scaling	Good	Better	Best
Process Complexity	Low	Medium	High
	Source: Adapted from Song et al (IEDM, 2021) with subsequent analysis by Applied Materials	Source: Adapted from public company disclosures (2021) with subsequent analysis by Applied Materials	Source: Adapted from Song et al (IEDM, 2021) with subsequent analysis by Applied Materials

APPLIED MATERIALS®

Frontside and Backside Wafer Fabrication

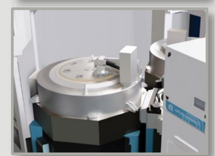
Broad Portfolio Addresses all Backside Power Distribution Schemes



Reflexion LK® Prime®
Silicon and Dielectric CMP

Producer® Eterna® FCVD™
Backside Isolation Fill

Centris® SYM3® Y
n-TSV Etch

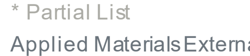


Olympia® ALD
n-TSV Isolation

IMS™ Metal Co-Optimized with CMP

- Silicide
- Contact Liner Fill
- Copper Barrier Seed

Reflexion LK Prime
New Metal CMP



Frontside and Backside Wafer Fabrication

Utilizing the backside of wafer for power delivery

New Ways to Integrate Chips

Sundar Ramamurthy
Group Vice President, GM
Semiconductor Products Groups

NEW WAYS TO WIRE AND PACKAGE CHIPS MASTER CLASS | May 26, 2022

Heterogeneous Chip Design – An Evolution of Moore's Law

Semiconductor Industry Revenue

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."
- Gordon Moore, 1965

Heterogenous integration

Flip-chip

Wire bonding

ERA 4: AI

ERA 3: Mobility

ERA 2: PC + Internet

ERA 1: Mainframe

Source: SEMI, VLSI, Applied Materials https://archive.computerhistory.org/resources/access/text/2017/03/102770822-05-01-acc.pdf

PC: Personal Computer
AI: Artificial Intelligence

Traditional Moore's Law Scaling Hits Limits

Microprocessor Trends

10^8
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0

Transistor (k)
Single thread performance (SpecINT x 1000)
Frequency (MHz)
Typical power (Watts)
Number of cores

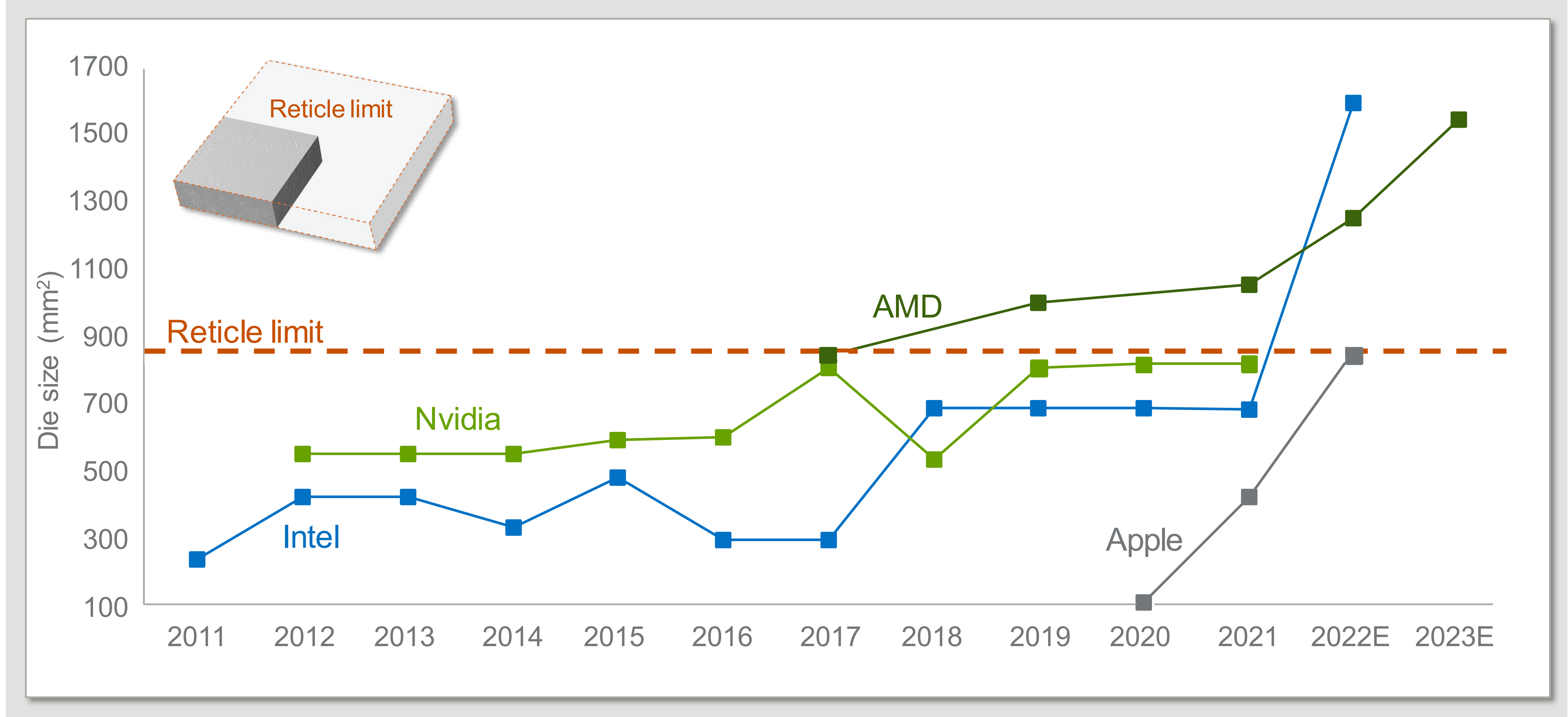
1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

- Single-threaded processor performance has plateaued despite increases in cores and transistors
- Application accelerator performance continues to scale with cores and transistors

Source: https://www.karlrupp.net/wp-content/uploads/2018/02/42-years-processor-trend.png
Source: Yole Développement Source: https://www.techspot.com/article/2143-ryzen-5000-ipc-performance/

MHz: Megahertz
SpecINT: computer benchmark specification for CPU integer processing power

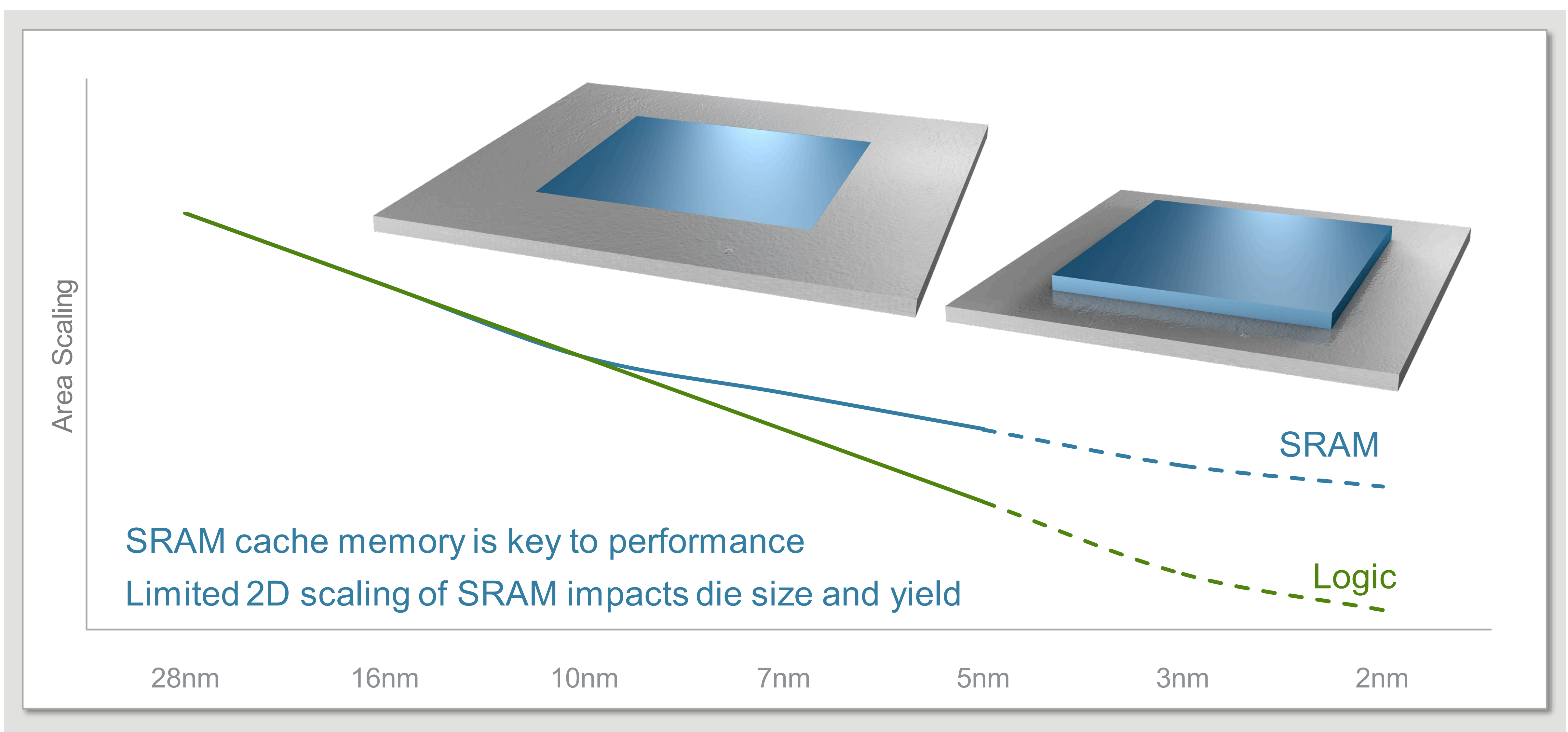
Transistor Counts are Hitting the Reticle Limit



Source: Jefferies

APPLIED MATERIALS®

Opportunity: Heterogeneous SRAM Integration



Source: Naffziger, VLSI Short Course, 2020
Source : Yole Développement

SRAM: Static Random Access Memory

Heterogenous Integration to the Rescue

GPU

CPU

Memory

RF

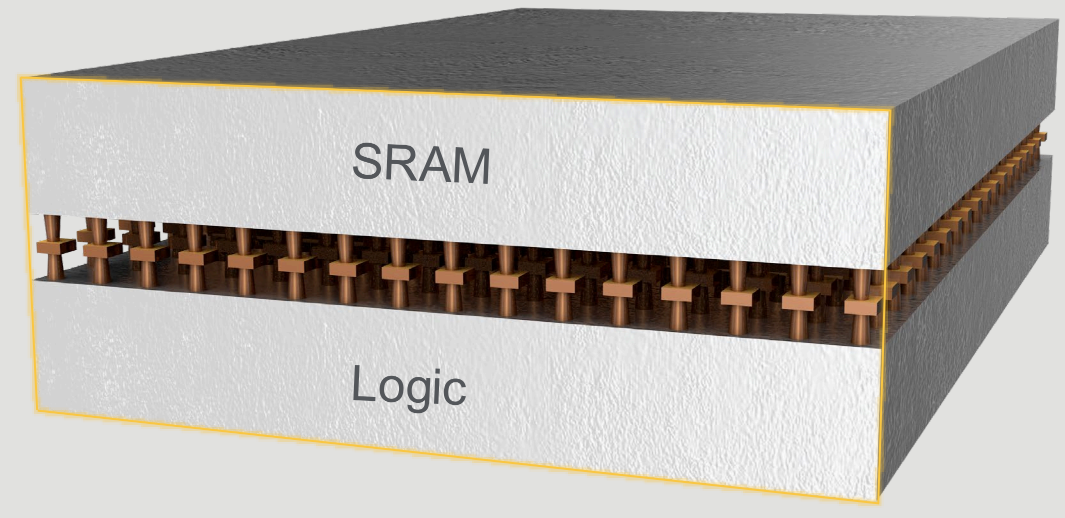
Image
Sensor

Heterogeneous integration enables logic, memory, sensors, power and communications
to be combined as a system-in-package

RF: Radio Frequency
GPU: Graphics Processing Unit
CPU: Central Processing Unit

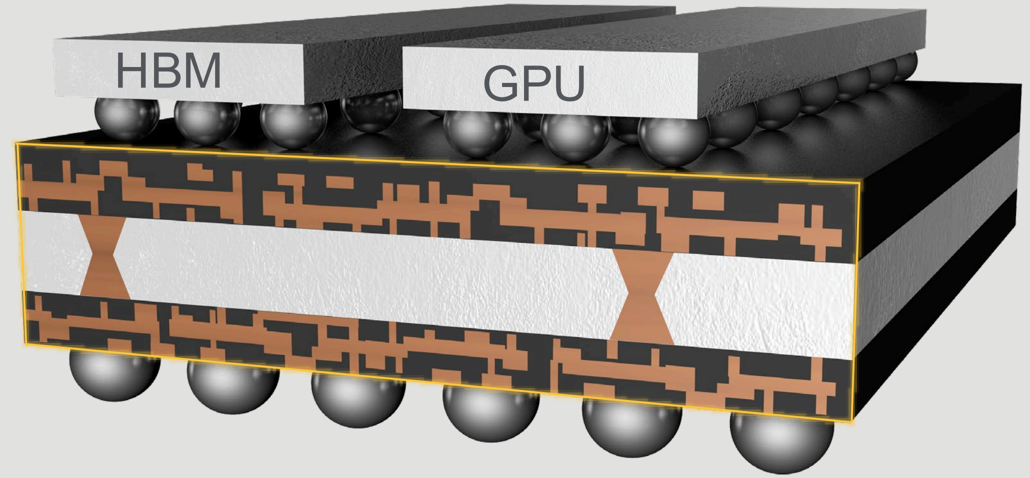
Advanced Interconnects Enable "System-in-Package" Era

Hybrid bonding



Hybrid bonding enables up to >10,000 I/Os per mm^2

Advanced substrates



Advanced substrates connect multiple high-performance die at high I/O density and data bandwidth

HBM: High bandwidth memory
I/O: Input / Output

Hybrid Bonding for High-Density Chip-to-Chip Interconnects

Hybrid bonding

Dielectric materials and copper pads fuse

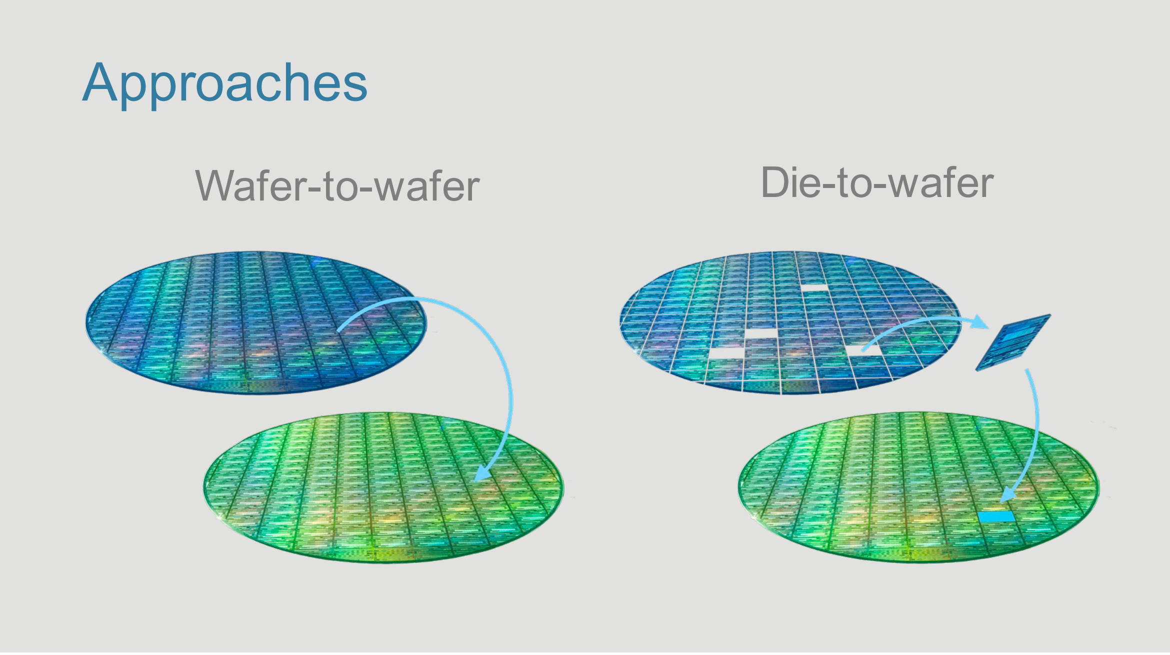
Chip 1

Chip 3

Chip 2

Multiple hybrid bonding options

Approaches

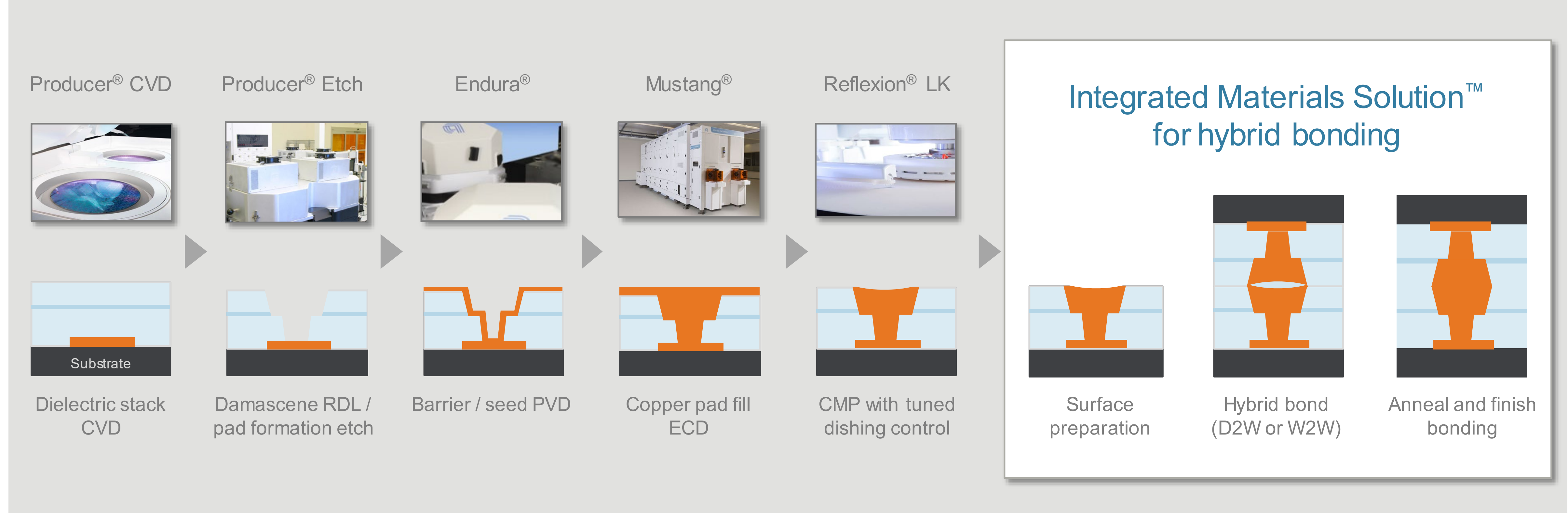


- Enables >10,000 connections per mm^2
- Requires precision in processing and alignment
- SoC performance can be reconstituted and expanded with hybrid bonded chiplets

SoC: System on a chip

APPLIED MATERIALS®

End-to-End Portfolio of Hybrid Bonding Solutions

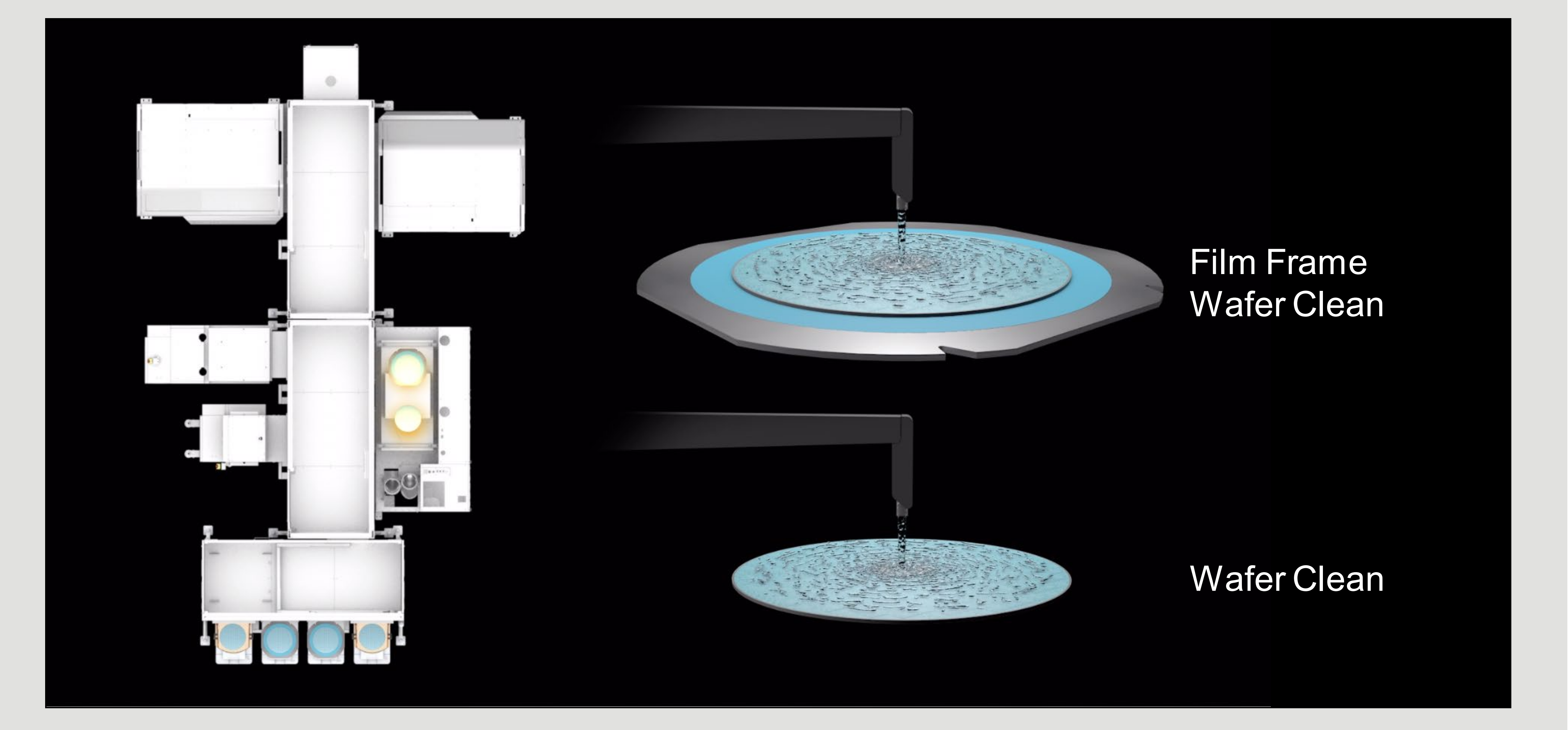


- Collaborating with partners to develop end-to-end technologies to ramp hybrid bonding solutions
- Center of Excellence investigates materials and process interactions on custom test vehicles

CVD: Chemical Vapor Deposition
RDL: Redistribution layer
PVD: Physical vapor deposition
ECD: Electrochemical deposition
CMP: Chemical mechanical polishing
D2W: Die to wafer
W2W: Wafer to wafer

APPLIED MATERIALS®

Integrated Materials Solution for Chip-to-Wafer Hybrid Bonding



UV: Ultraviolet

APPLIED MATERIALS®

Advanced Substrates Improve I/O Density and Power

10,000
1,000
100
10
1

I/O per mm²

1000
100
10
1

Line/space pitch (μm)

Wire bond substrates

1-10 I/O/mm²
>10 pJ/bit

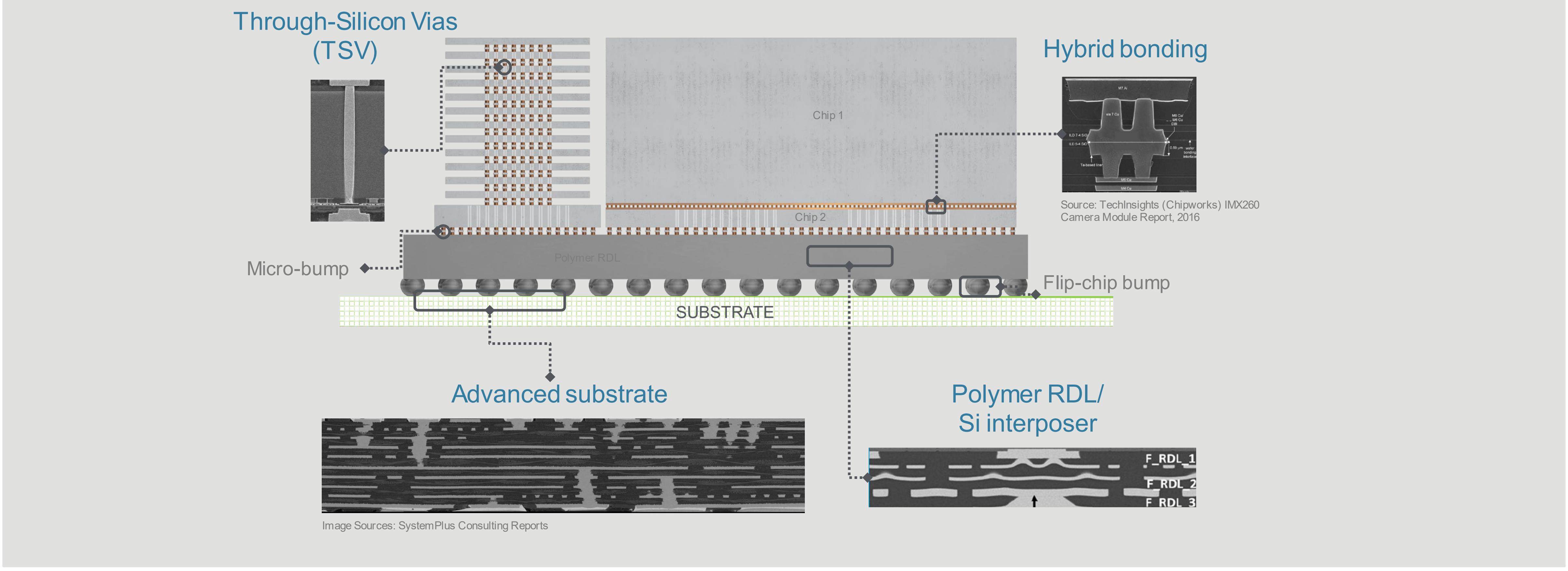
Flip-chip substrates

100-500 I/O/mm²
>1 pJ/bit

Advanced flip-chip substrates

>1,000 I/O/mm²
<0.1 pJ/bit

System Integration with Emerging 2D and 3D Interconnects

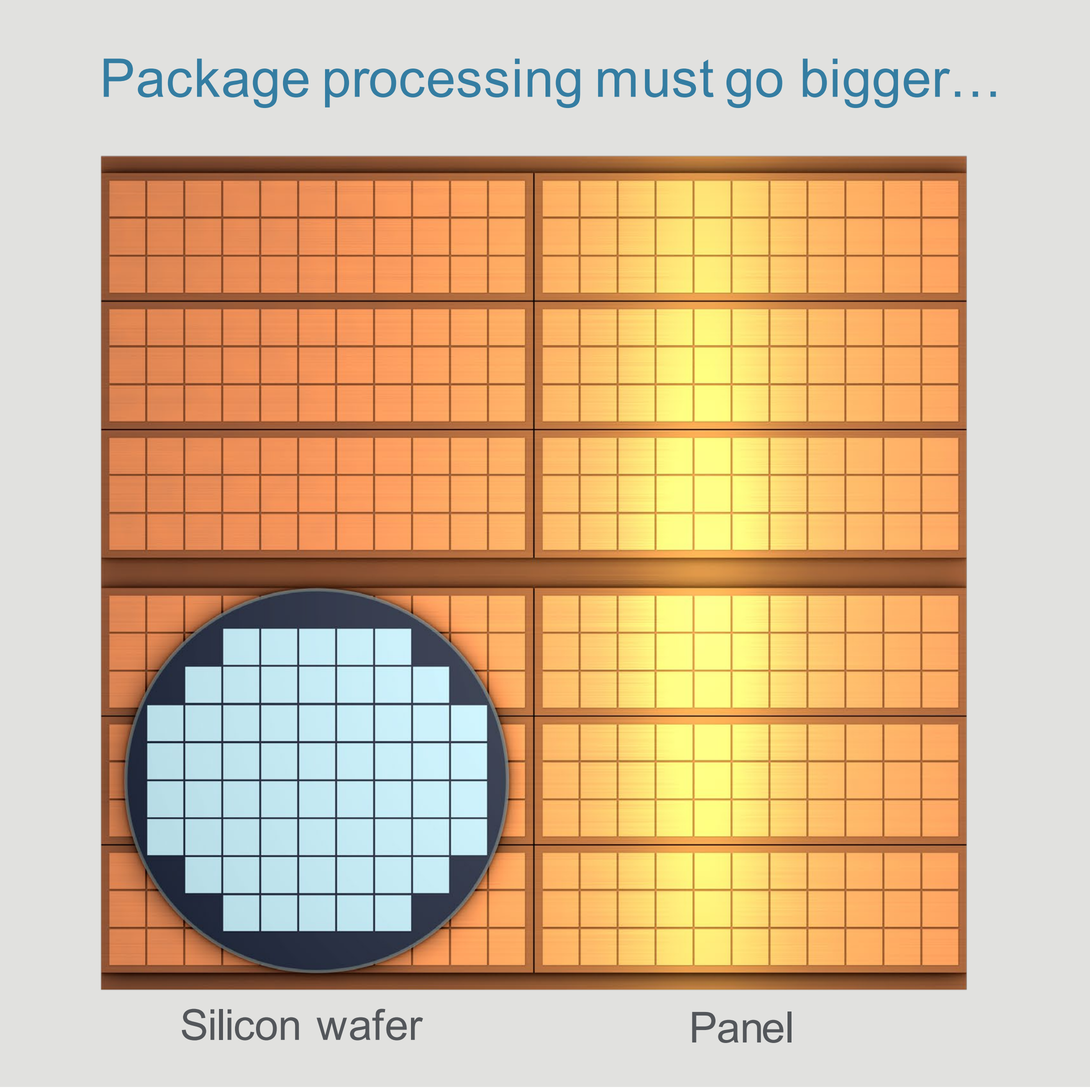


- Advanced substrates package chips side-by-side with higher bandwidth (more I/Os) and lower power
- TSVs with micro-bumps or hybrid bonding create vertical interconnects allowing chip-on-chip stacking

APPLIED MATERIALS

Quest for Performance is Making Packages Larger

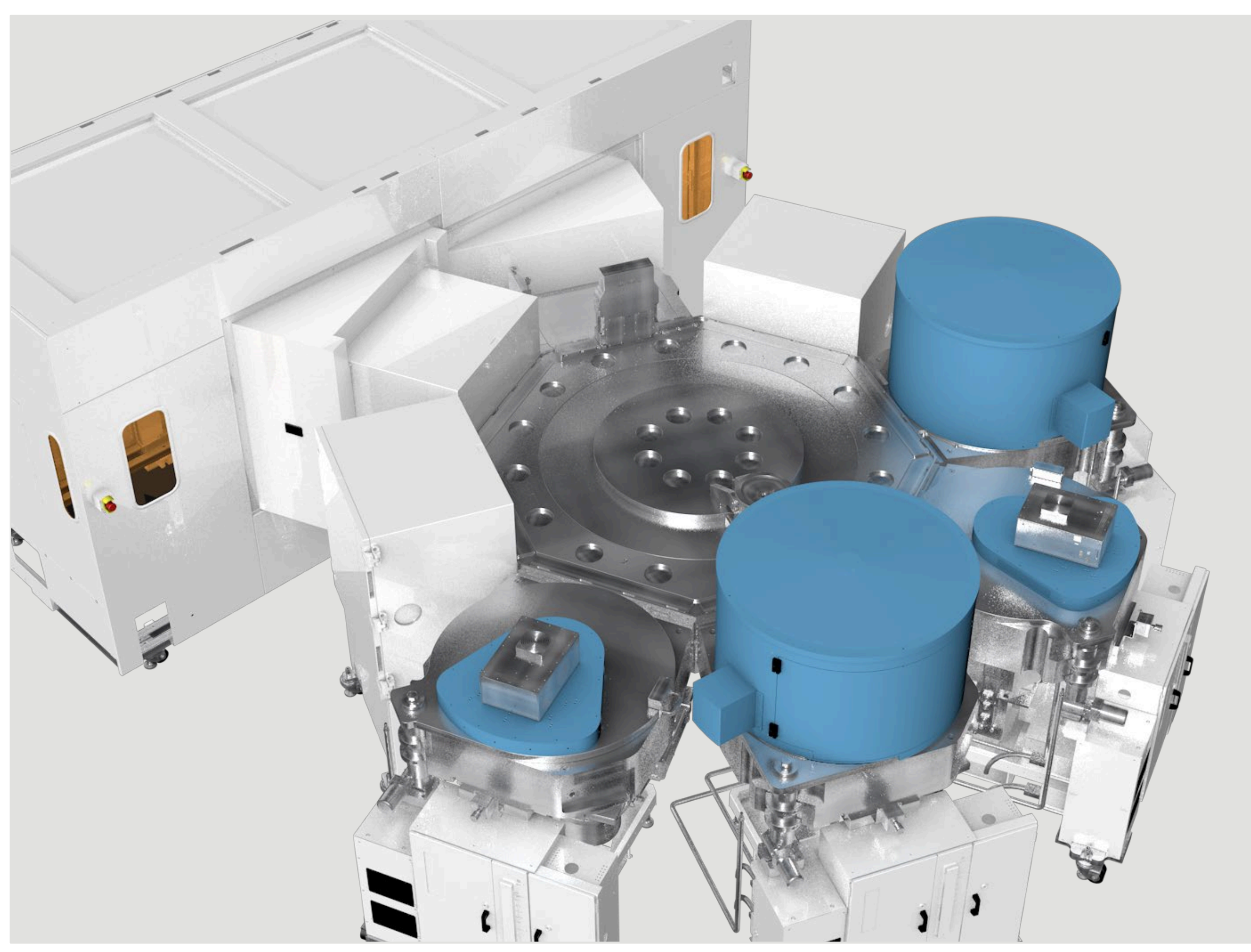
Package processing must go bigger…



- Multiple chiplets in a package
- Package areas as large as 10,000mm^2
- Round wafers have poor area efficiency

Panels enable greater number of larger packages

Semiconductor-Grade Large Substrate Processing



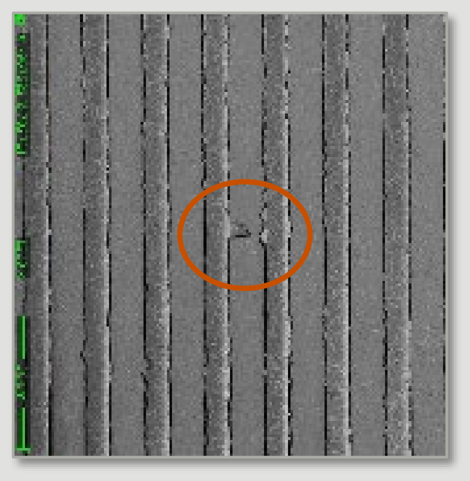
Applied Topaz™ PVD System

- Substrates up to 600x600mm
- Cluster chamber architecture
- Multiple applications supported

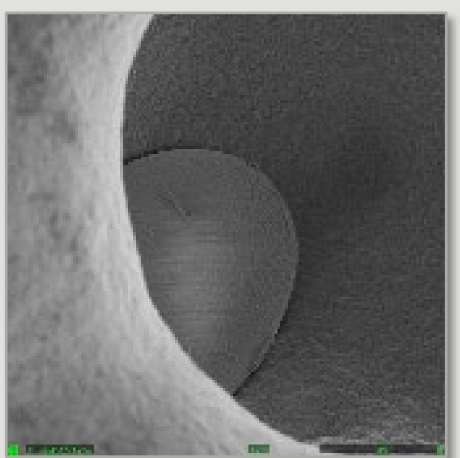
Creating an industry ecosystem for semiconductor-grade panel-level packaging

Panel-Level eBeam Metrology and Test

Defect review with SEM and FIB analysis



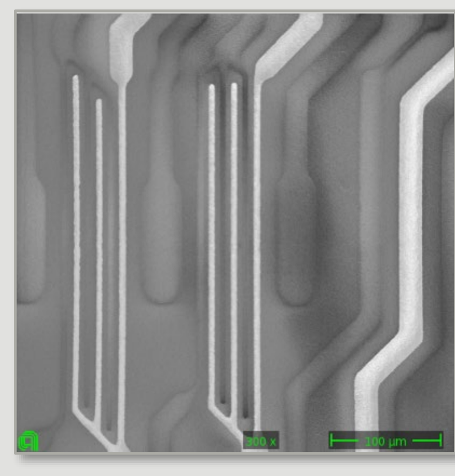
Protrusion



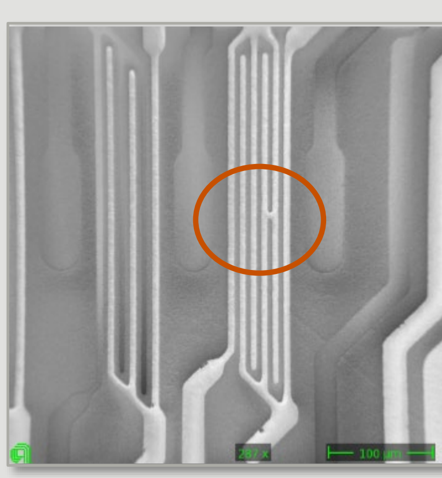
Residuals

- Automatic defect review
- Precise CD measurement
- In-situ failure analysis

Non-destructive eBeam test



Normal interconnect

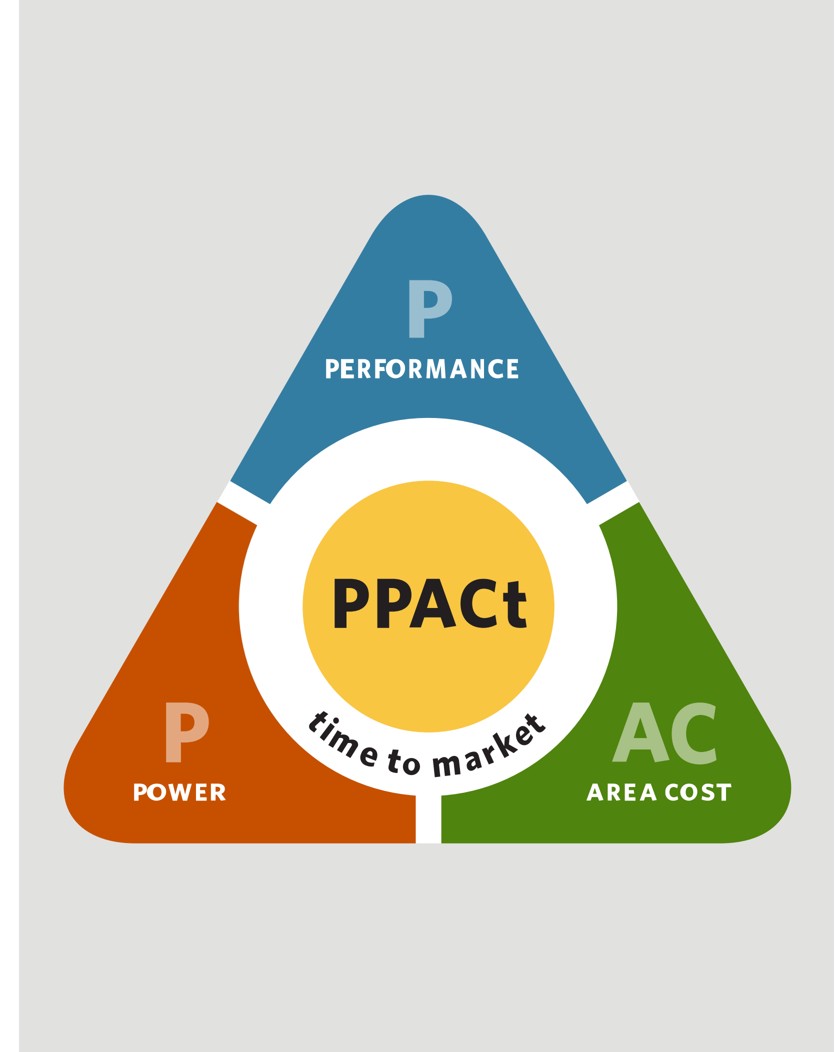


Shorts highlighted

- Fault detection by voltage contrast
- High-throughput analysis
- Damage-free

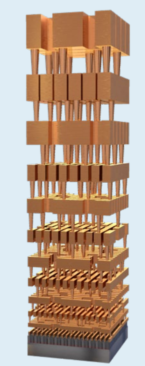
eBeam: Electron beam
SEM: Scanning electron microscope
FIB: Focused ion beam

Wiring & Heterogenous Integration Enable PPACt™ Scaling



Low-resistance contacts and interconnects

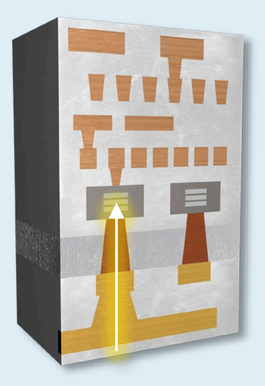
- P Lower power loss
- P Faster switching



40-50% resistance reduction @ 3nm with IMS™

Backside power distribution networks

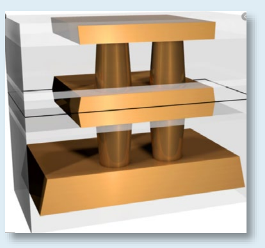
- AC Increased logic scaling
- P Lower power loss



Up to 30% logic density improvement vs. frontside power

Hybrid bonding and advanced substrates

- t Heterogenous integration
- P Higher I/O and bandwidth
- P Lower power loss



Enables >10,000 I/Os per mm^2 and packages as large as $10{,}000mm^2$

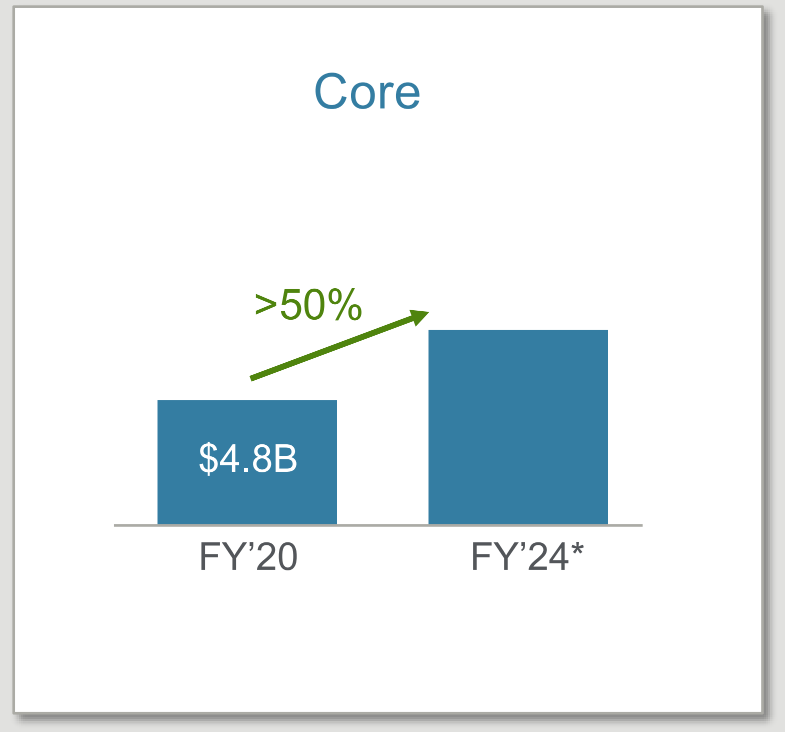
IMS: Integrated Materials Solution

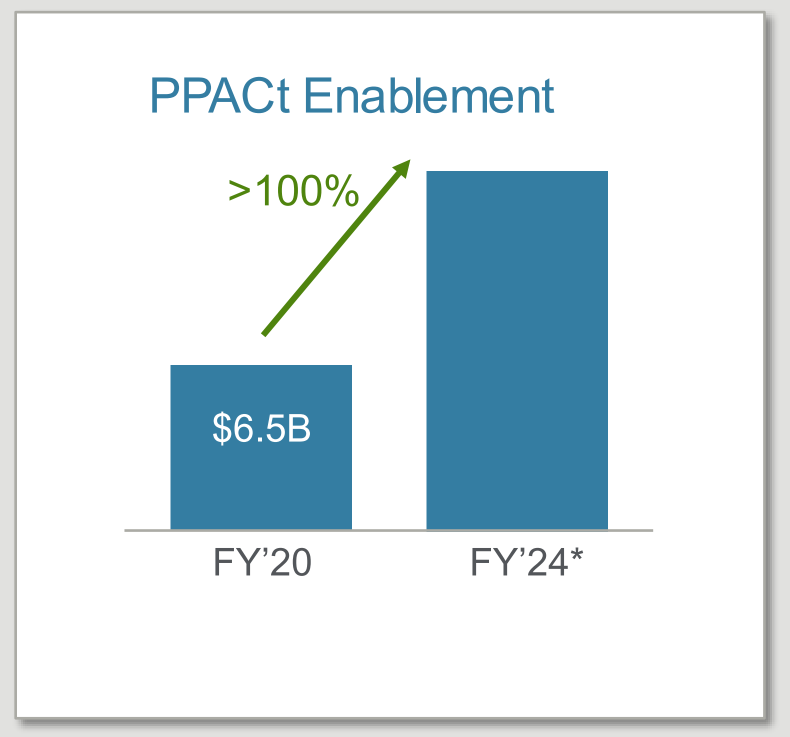
Growth in Chip Wiring and Integration

Raman Achutharaman, Ph.D.
Group Vice President
Semiconductor Products Group

NEW WAYS TO WIRE AND INTEGRATE CHIPS MASTER CLASS | May 26, 2022

Semi Systems Revenue Growth Drivers





*Represents 2024 Financial Model High Scenario

The New Playbook

PERFORMANCE

POWER

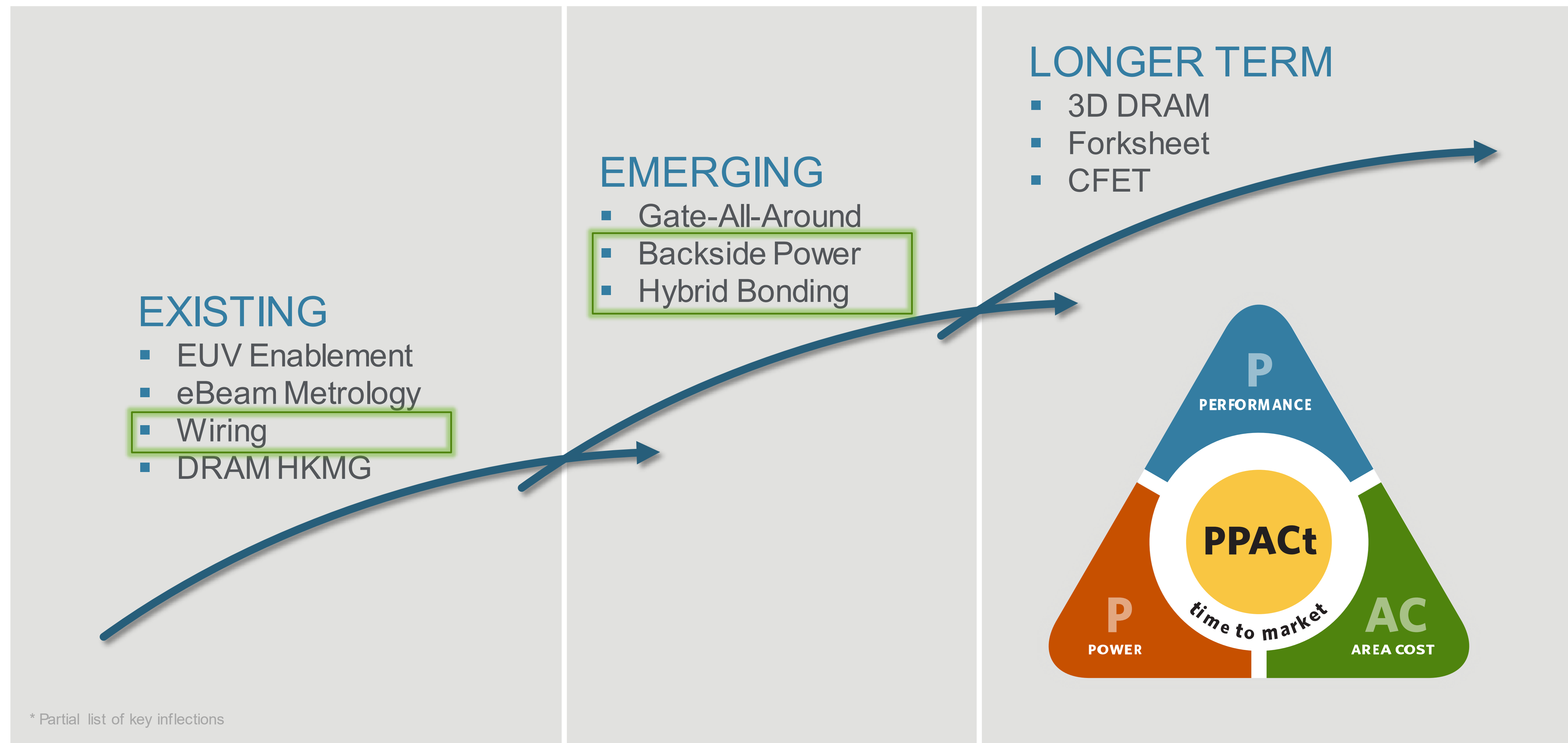
AREA COST

PPACt

time to market

ENABLED BY	KEY INFLECTIONS
New architectures	New ASICs and accelerators; New memory / in-memory compute; Specialty, CIS, power
New structures / 3D	GAA transistors; Backside power distribution; 3D NAND, 3D DRAM
New materials	Gate; Contact; Interconnect
New ways to shrink	EUV enablement; Materials-enabled patterning; 3D patterning control
Advanced packaging	High-bandwidth memory; 2.5D silicon interposer; 3D TSV, hybrid bonding

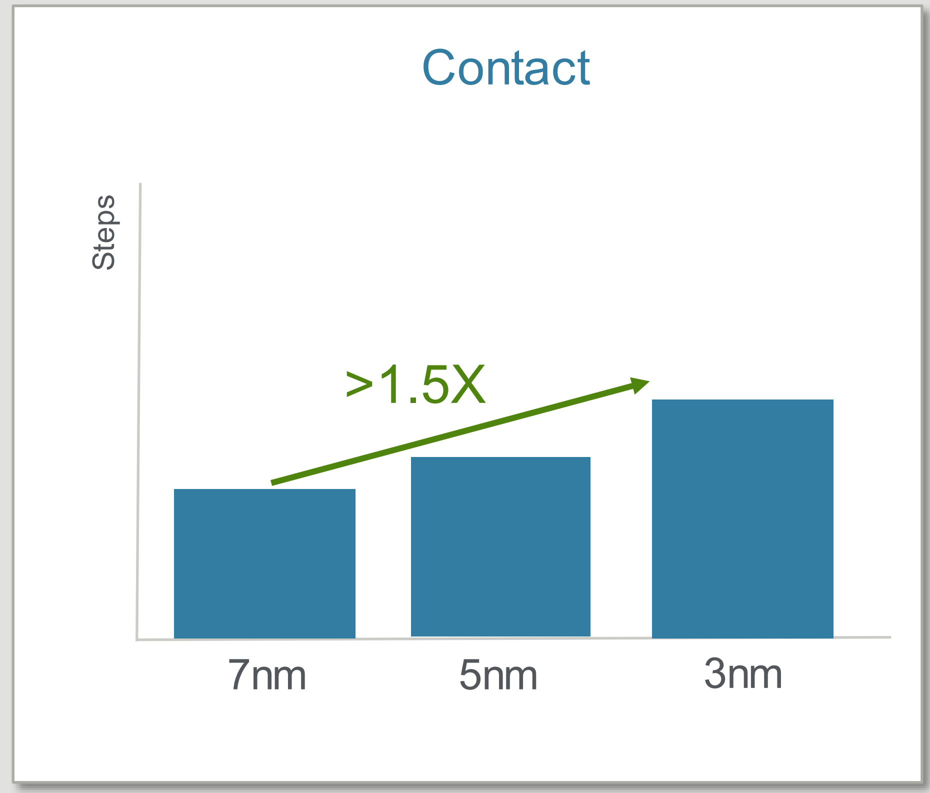
Inflections Over Time

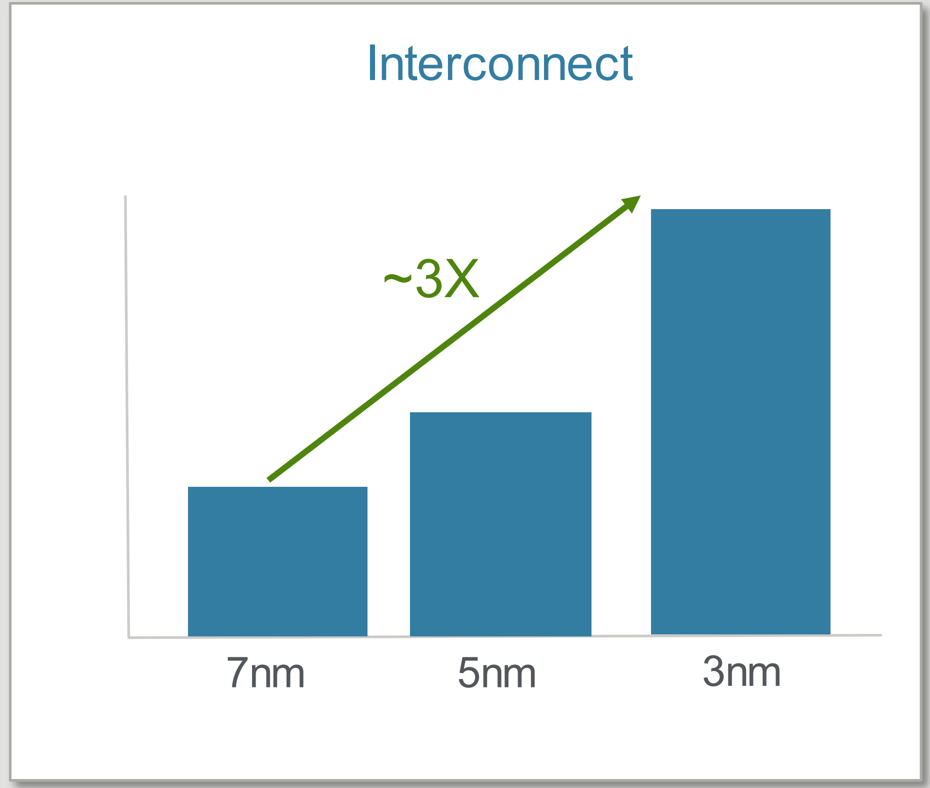


APPLIED MATERIALS

Wiring Growth Opportunity

Expect to grow wiring revenue at ~3X the rate of WFE 2020→2024



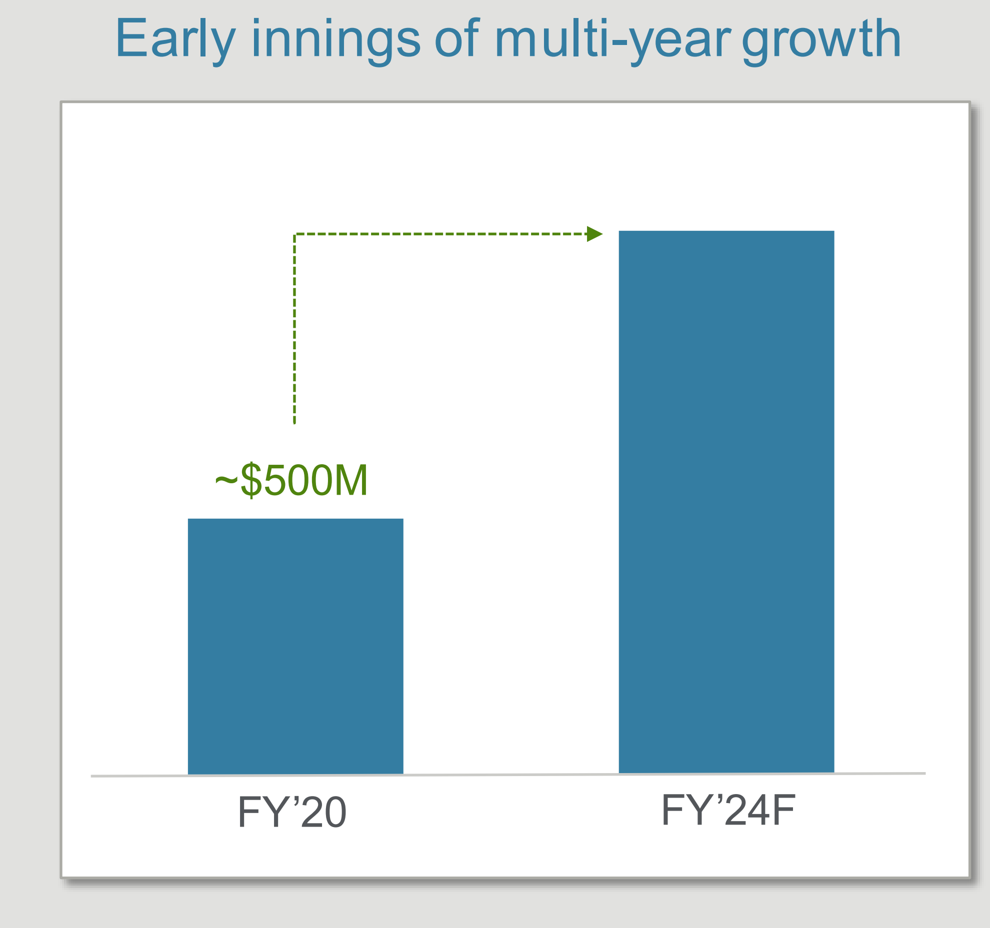


Applied's wiring opportunity increases by >$1B from 7nm→3nm

*Leading Foundry/Logic Customers

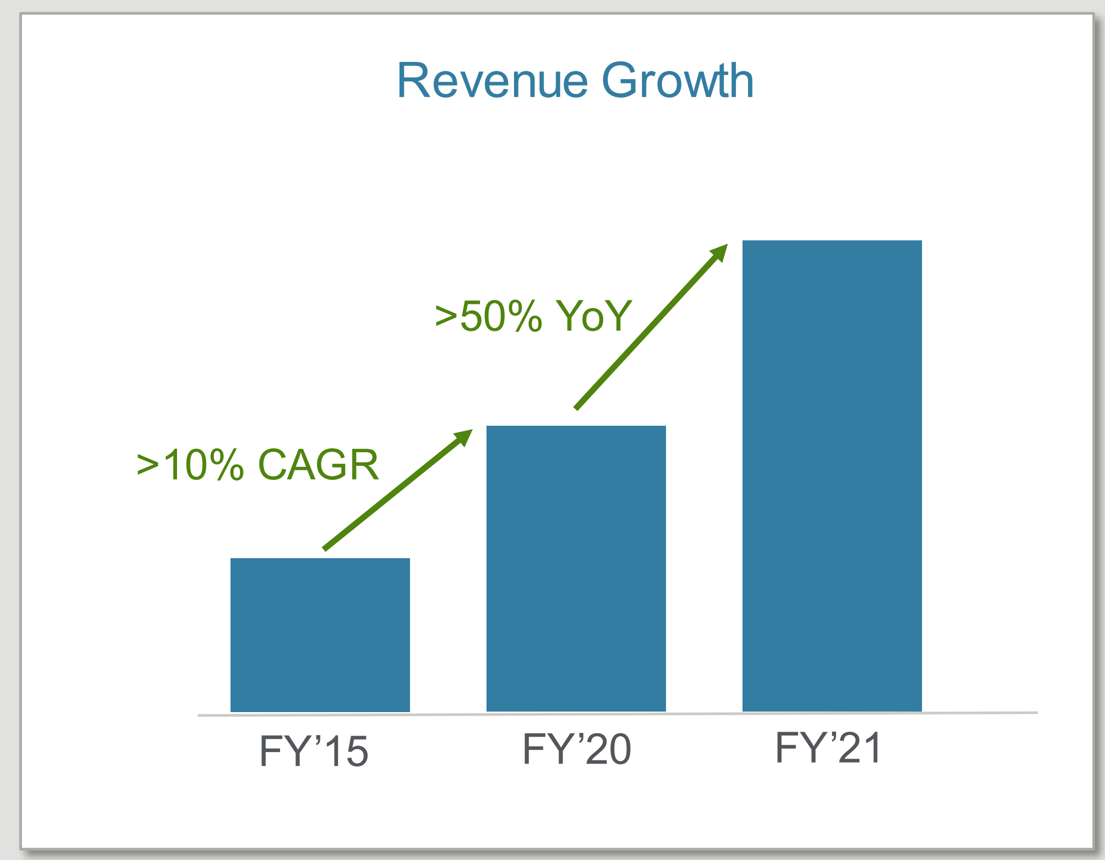
Positioned for Growth in Packaging

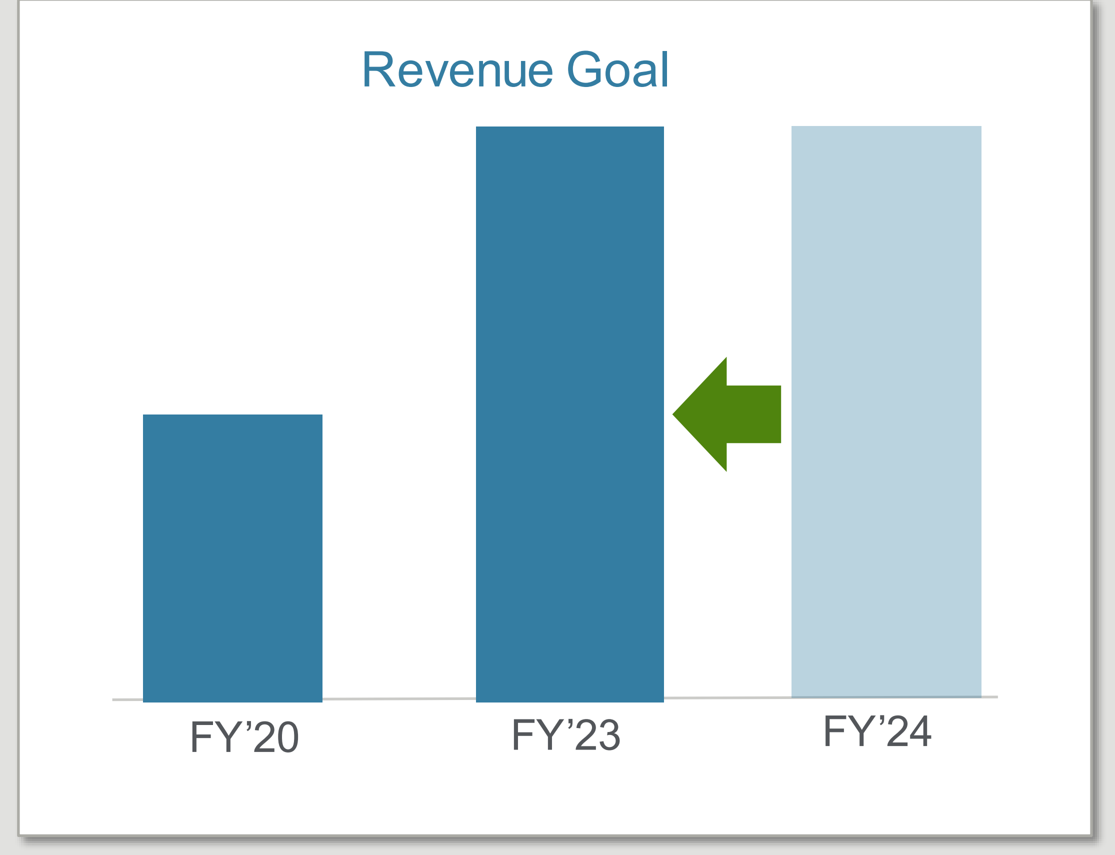
Early innings of multi-year growth



- #1 in bond pad, bump and TSV
- Broad product portfolio + full-flow lab
- Key ecosystem partnerships
- Delivering system level PPACt gains: ↓ R, ↓ power, ↓ area, ↑ performance

Packaging Growth Opportunity



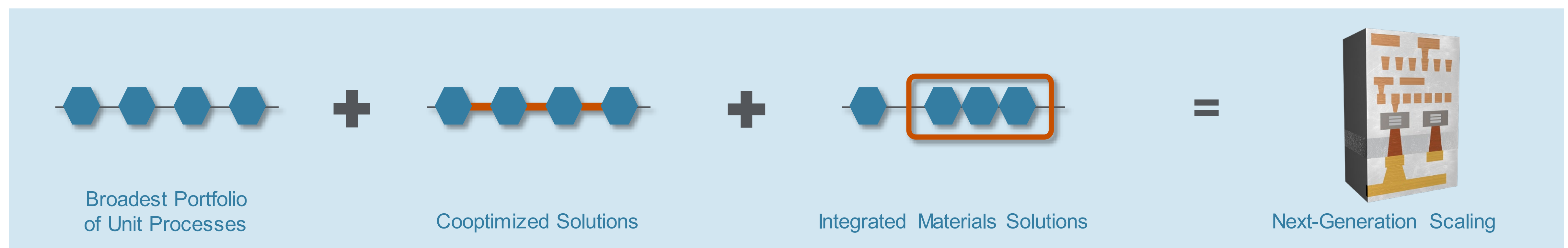


Packaging Portfolio

Future

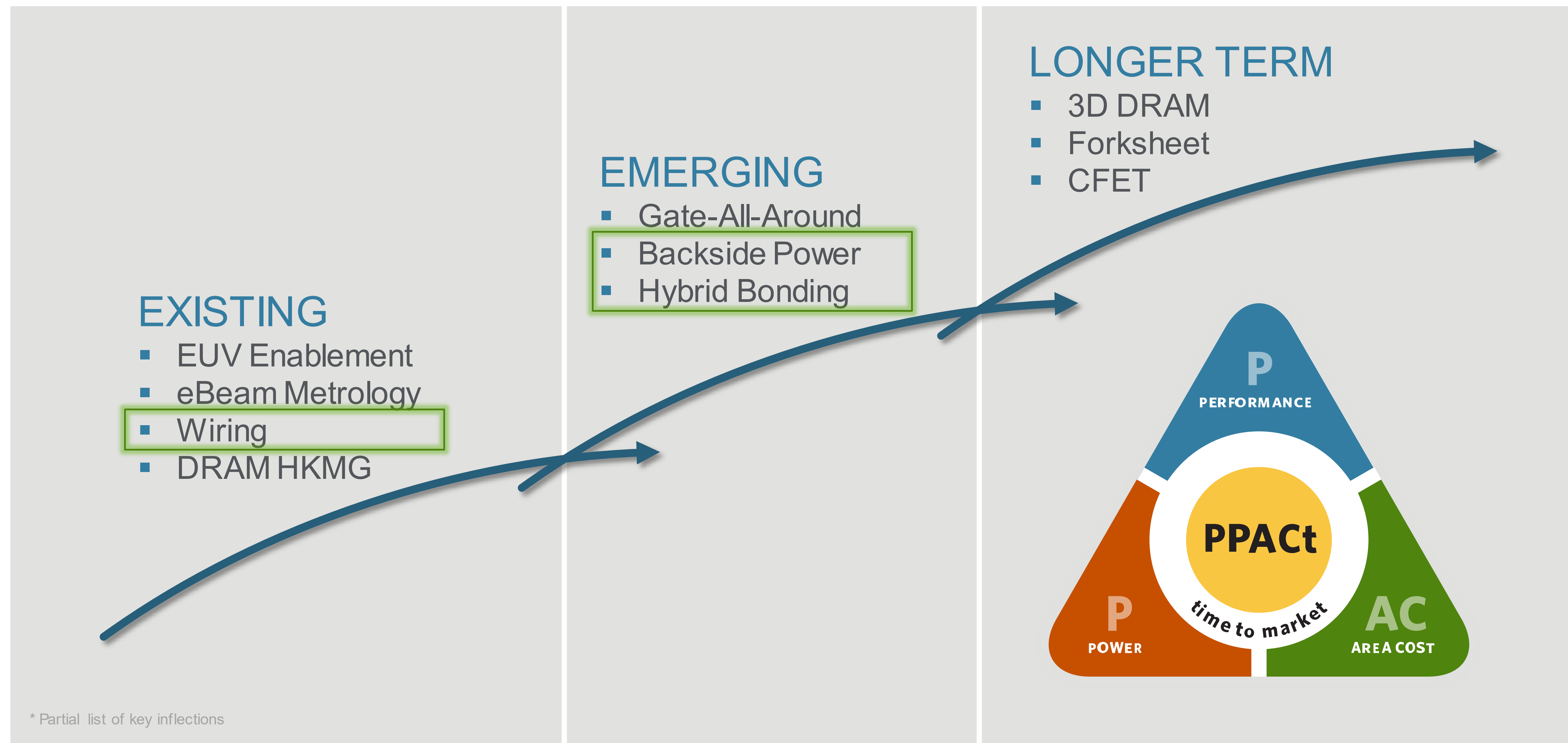
- Integrated Materials Solution for hybrid bonding
- Large-area metrology and process control

Broad Portfolio Addresses all Backside Power Distribution Schemes



Buried Power Rail	Power Via	Backside Contact to S/D	Backside Power Delivery Approaches
Low	Medium	High	Logic Density, Process Complexity

Inflections Over Time



APPLIED MATERIALS®

APPLIED
MATERIALS®
make possible