2025 SEMICON WEST

Technology Breakfast

APPLIED MATERIALS

Forward Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market positions, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including changes in interest rates and prices for goods and services; the implementation of additional export regulations and license requirements and their interpretation, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies and our ability to obtain licenses or authorizations on a timely basis, if at all; imposition of new or increases in tariffs and any retaliatory measures, including their impact on demand for our products and services; the effects of geopolitical turmoil or conflicts; demand for semiconductor chips and electronic devices; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of regional or global health epidemics; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-K, 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

From Atoms to AI

Kevin Moraes, Ph.D.

Vice President, Semiconductor Products Group

OCTOBER 7, 2025


SEMICON®
2025
WEST

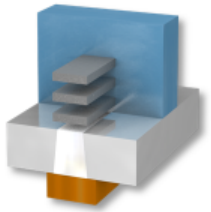
2024 Tech Breakfast in San Francisco

Key Takeaways from 2024 Tech Breakfast

Materials Engineering-Enabled Technology Inflections

High-Performance Logic

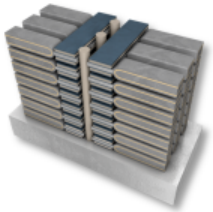
Gate-All-Around
Density +20%, energy efficiency +30%



Backside Power Delivery
Density +30%, energy efficiency +20%

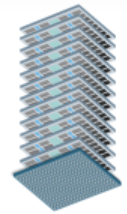
Compute Memory

Planar DRAM Scaling
Density +30%, energy efficiency +15%

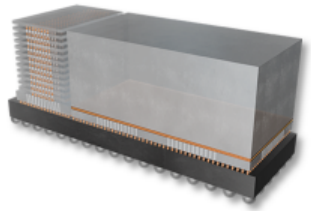


3D DRAM
Density +30% energy efficiency 15%

Advanced Packaging



High-Bandwidth Memory
Density +250%, bandwidth +1,000%



Heterogeneous Integration
Volumetric scaling, lower power

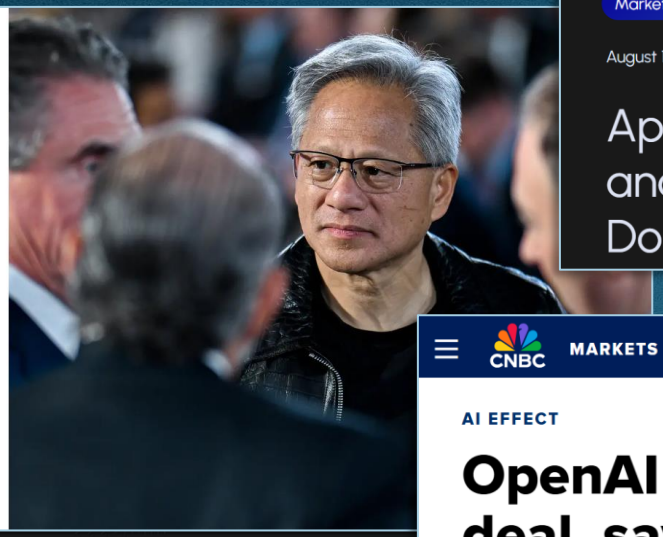
Helping deliver 10,000X improvement in energy-efficient performance by 2040

AI's Rapid Evolution

The New York Times

Nvidia to Invest $100 Billion in OpenAI

The chipmaker's investment in the San Francisco start-up is an indication of the wild financial figures being tossed around in the world of artificial intelligence.



Futurum

Market Coverage | News

August 14, 2025 Ray Wang

Applied Materials' New Partnership with Apple and Texas Instruments Aims to Enhance Domestic Innovation and Supply Chain

CNBC MARKETS BUSINESS INVESTING TECH POLITICS VIDEO INVESTING CLUB JOIN PRO JOIN

AI EFFECT

OpenAI expands Oracle data center deal, says parts of Stargate 1 in Texas are operational

PUBLISHED TUE, JUL 22 2025•10:09 AM EDT

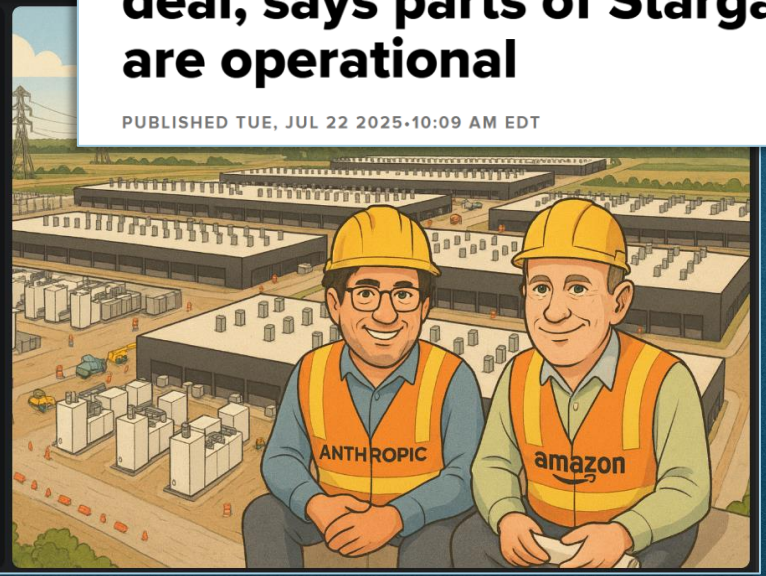
September 3, 2025

Amazon's AI Resurgence: AWS & Anthropic's Multi-Gigawatt Trainium Expansion // Anthropic multi-gigawatt clusters, Trainium ramp, best TCO per memory bandwidth, system-level roadmap, Bedrock and internal models

14 minutes

5 comments

By Jeremie Eliahou Ontiveros, Dylan Patel, AJ Kourabi and Myron Xie



APPLIED MATERIALS

AGENDA

7:30 Prabu Raja, Ph.D.
Energy-Efficient AI at Scale

7:40 Jim Chambers, Ph.D.
NVIDIA
Accelerated Computing and Semiconductor Ecosystem: The Virtuous Cycle

7:55 Rose Castanares
TSMC
Industry Needs to Enable AI Everywhere

8:10 Mukund Srinivasan, Ph.D.
Enablement

8:15 Enablement Expert Panel

- » Bala Haran, Ph.D. — Silicon Enablement
- » Subi Kengeri — Package Enablement
- » Mike Chudzik, Ph.D. — Fab R&D Enablement
- » Steve Frezon — Fab Ramp Enablement

8:50 Prabu Raja, Ph.D.
Growing our Opportunity and Share

PRESENTATIONS ARE POSTED AT
https://ir.appliedmaterials.com/events

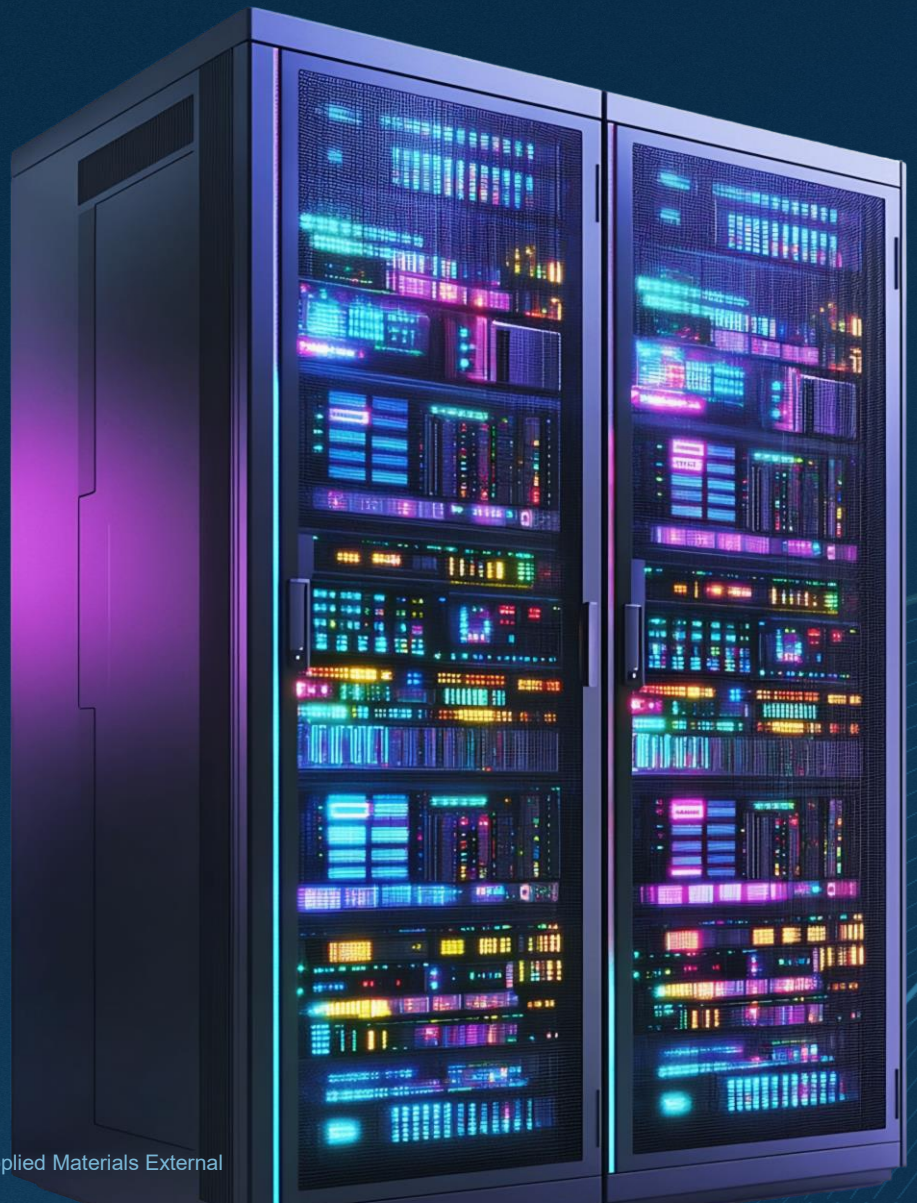
Energy-Efficient AI at Scale

Prabu Raja, Ph.D.

President, Semiconductor Products Group

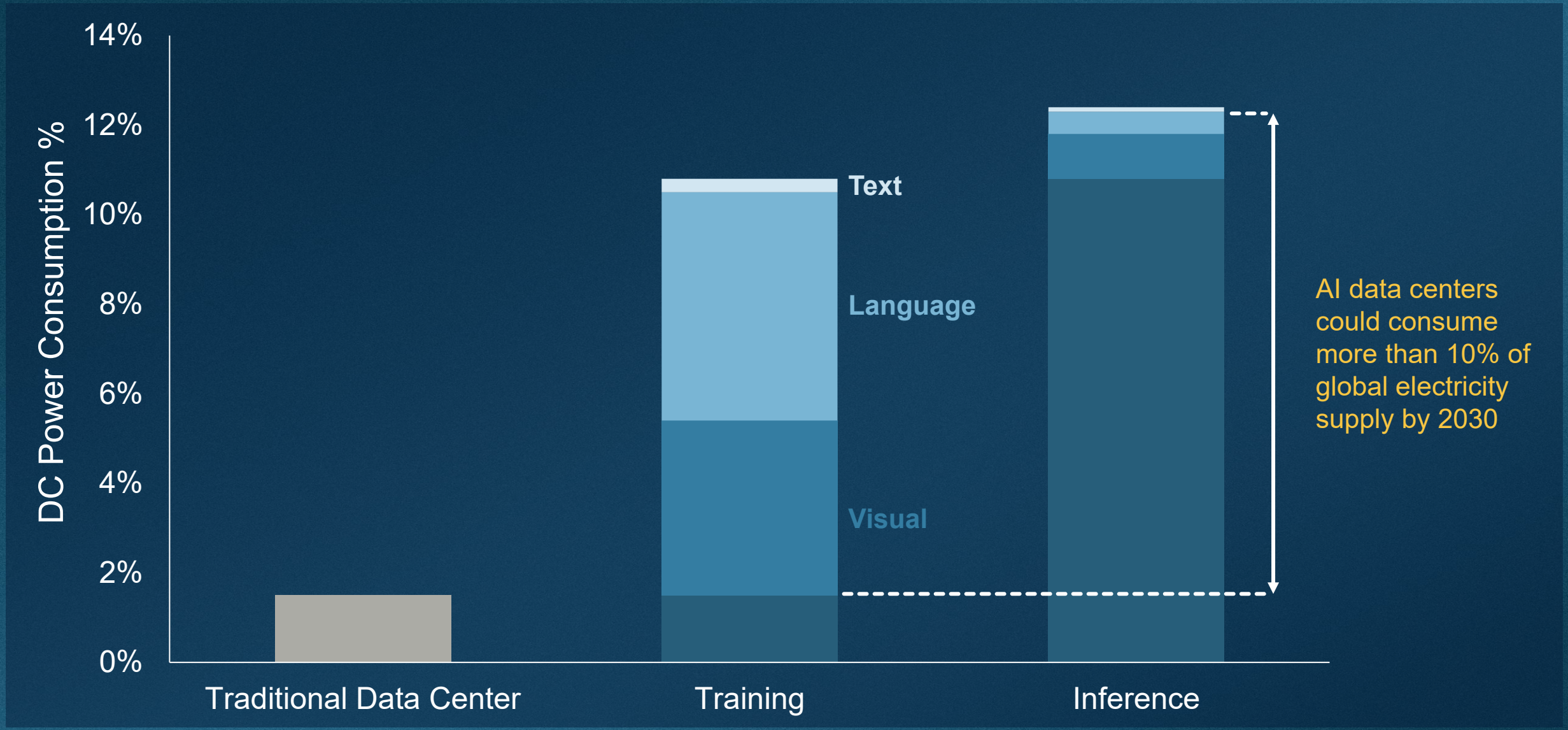
OCTOBER 7, 2025

NOW:
AI Intelligent Cloud



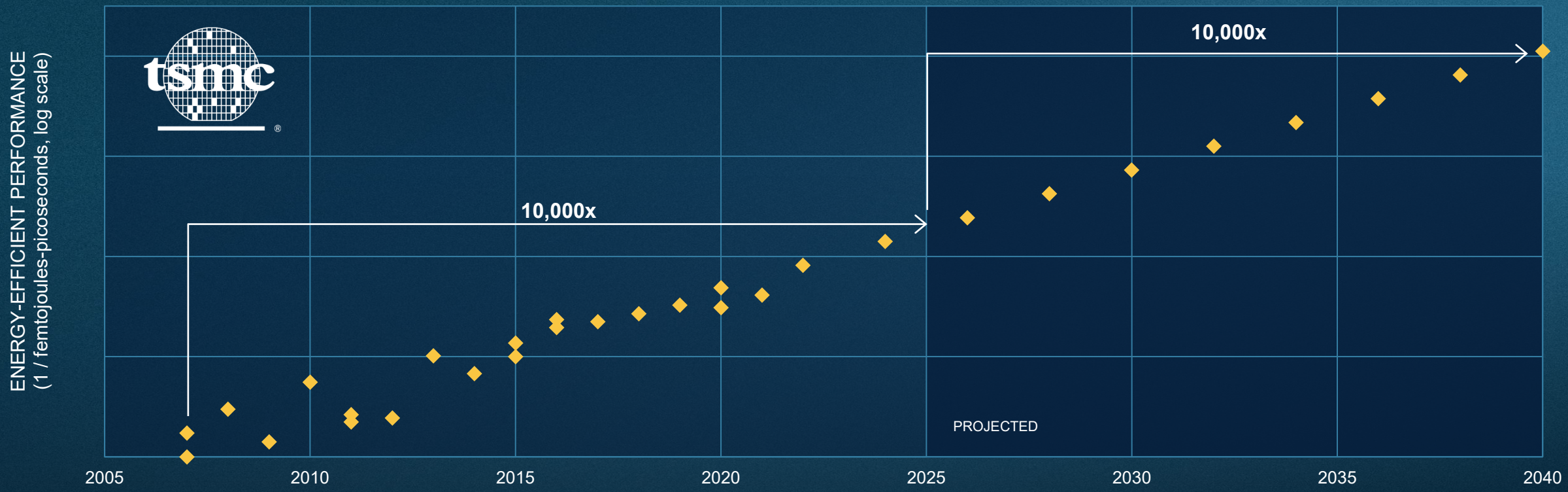
FUTURE:
AI Intelligence Everywhere!

AI Scaling Faces an Energy Consumption Problem



Source: Applied Materials

10,000x Improvement Needed in Next 15 Years



Global Race for AI Leadership Determined by Energy-Efficient Computing Performance

Source: Mark Liu and H.-S. Philip Wong, IEEE Spectrum, March 28, 2024. https://spectrum.ieee.org/trillion-transistor-gpu

Semi Devices Foundational for Energy Efficient Performance

Leading-edge Logic

High-performance DRAM

High-bandwidth DRAM

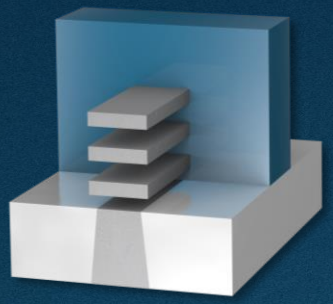
Advanced Packaging

Power semi (ICAPS)

ICAPS: Internet of Things, Communications, Automotive, Power and Sensors

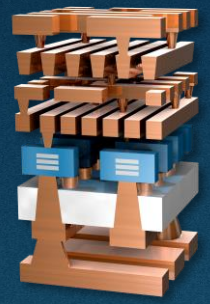
New 3D Architecture Inflections Offer Big EEP Improvements

AI Leading-edge Logic



GAA Transistor

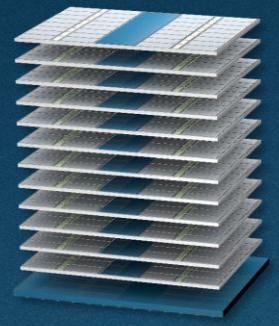
30% ↓ power,
15% ↑ performance



Backside Power

30% ↑ density
↑ 10% performance

AI DRAM: HBM + Leading Edge

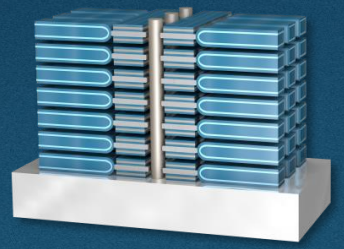


High Bandwidth Memory

Bandwidth +1,000%

Vertical Transistor

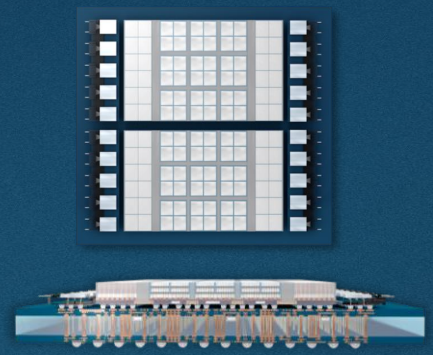
EEP +15%



3D DRAM

EEP +15%

AI Sys. Integration



Advanced Packaging

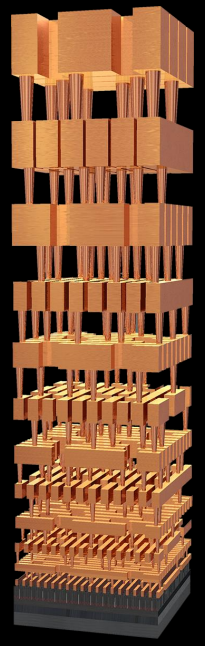
1000x ↑ IO / mm²
10x lower pJ / bit ↓

Helping deliver **10,000X EEP improvement** by 2040

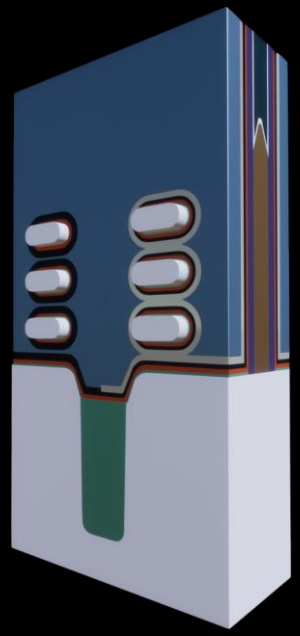
IO: input/output, EEP: energy-efficient performance

Inflection Complexity: Gate-All-Around Transistor Example

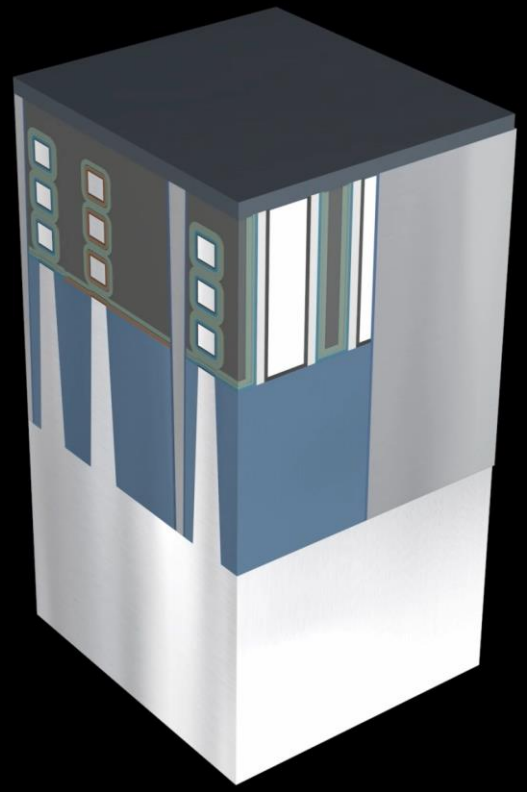
Copper wiring
>15 layers
>100km length



>2,000
PROCESS STEPS



>500
FOR GAA TRANSISTOR



More Steps
More Materials
More Interfaces
More Step-to-Step Interactions

Step-to-Step Interactions Challenges

(GAA contact)

Clean

Deposition hardmask

Deposition patterning film

Track photoresist

Lithography trench pattern

Lithography contact pattern

Etch patterning film open

Etch hardmask open

Etch inter-layer dielectric oxide

Ash/etch patterning films

ALD liner deposition

Etch source-drain cavity shaping

Epitaxial contact deposition

Silicide deposition and anneal

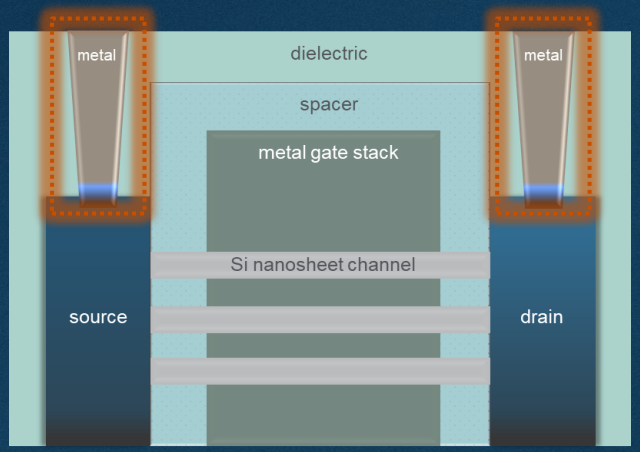
Metal cap deposition

Treatment

Metal fill

CMP metal overburden removal

Contact Module



Requires MAGIC WITH MATERIALS

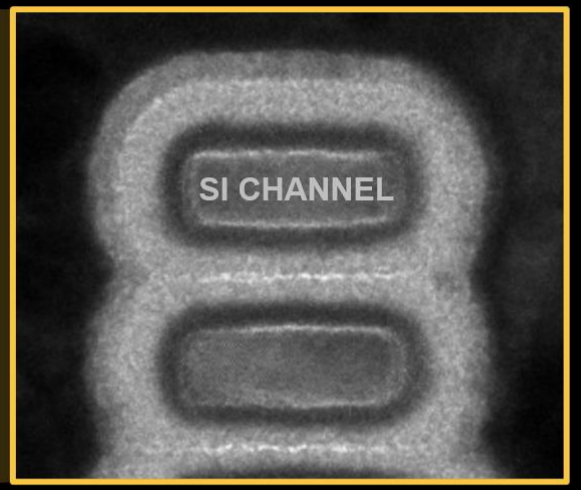
High Process Complexity from **Interfaces**

Silicon nanosheet

Gate oxide

Metal gate

10nm

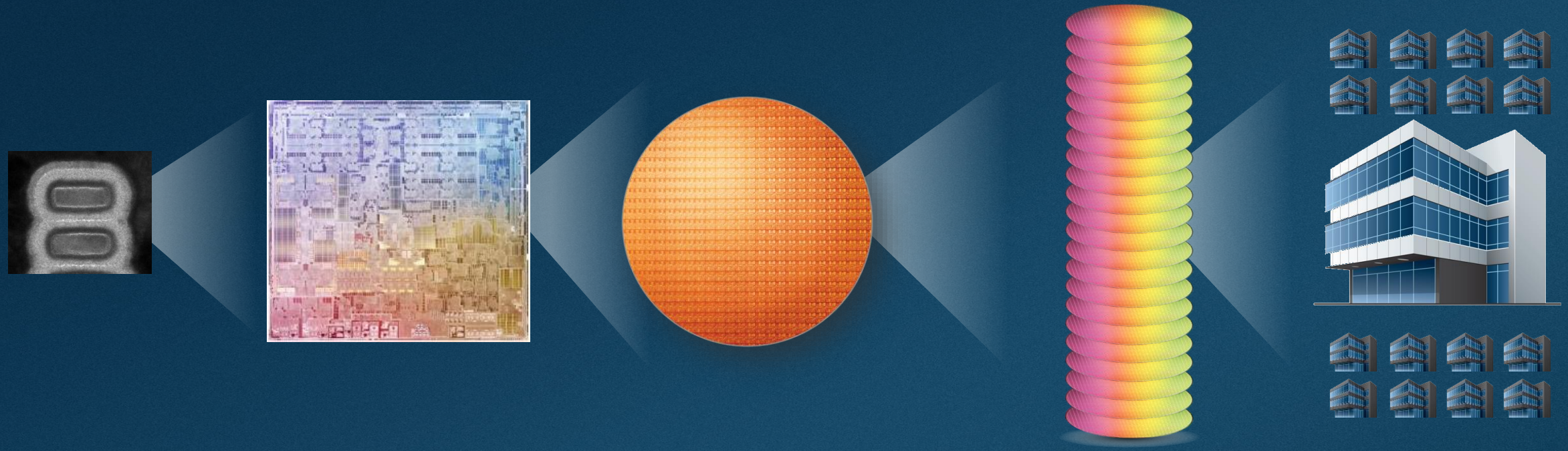


In just **~10nm** between nanosheets

- **>5** distinct materials
- **1-2nm** per layer of material
- **1Å precision required**

APPLIED MATERIALS

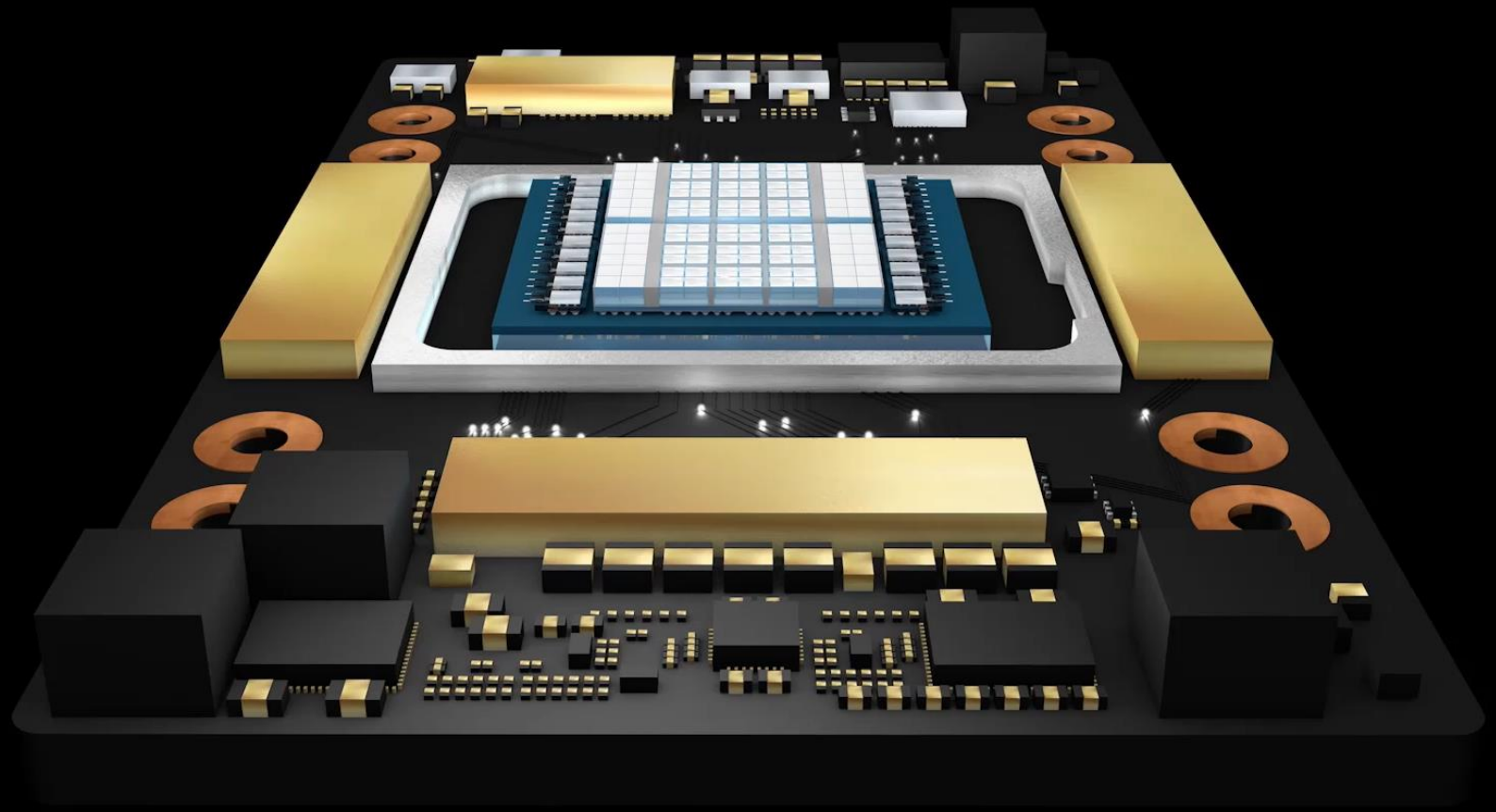
Complexity: Atomic-level Processing at Industrial Scale



Transistor stack level (1Å precision)	Die Level (mm scale)	Wafer Level (300mm)	Fab Scale	**Industrial Scale**
3 Transistors	X **~20B Transistors**	X **~400 dies / wafer**	X **100,000 wafers per month Giga fab**	X **~25 fabs**

6 X 10^{19} with 1Å precision transistors per year needed

Advanced Packaging
Complexity also Increasing

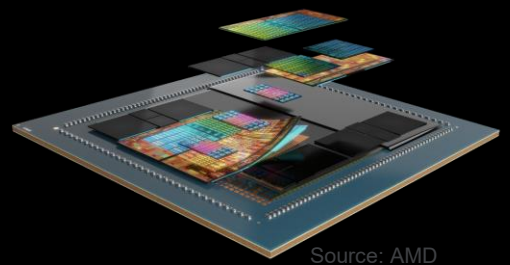


Connects

117 Chips in 1 package

>10 Million

3D connections



Source: AMD

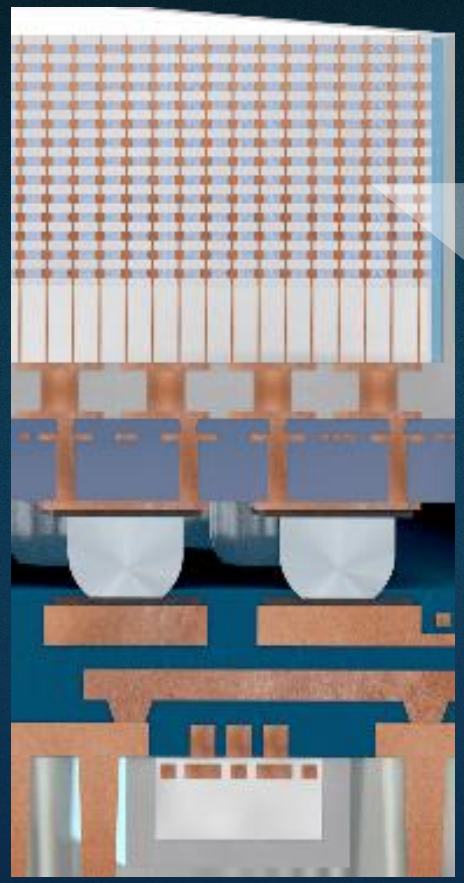
>1.4M Hybrid Bonds

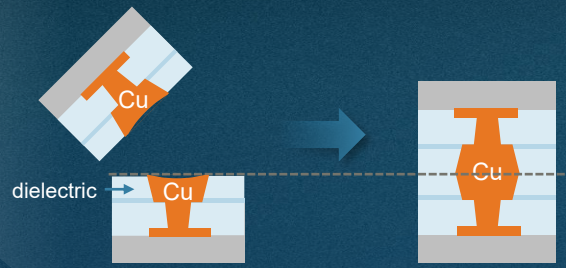
>2.9M TSVs

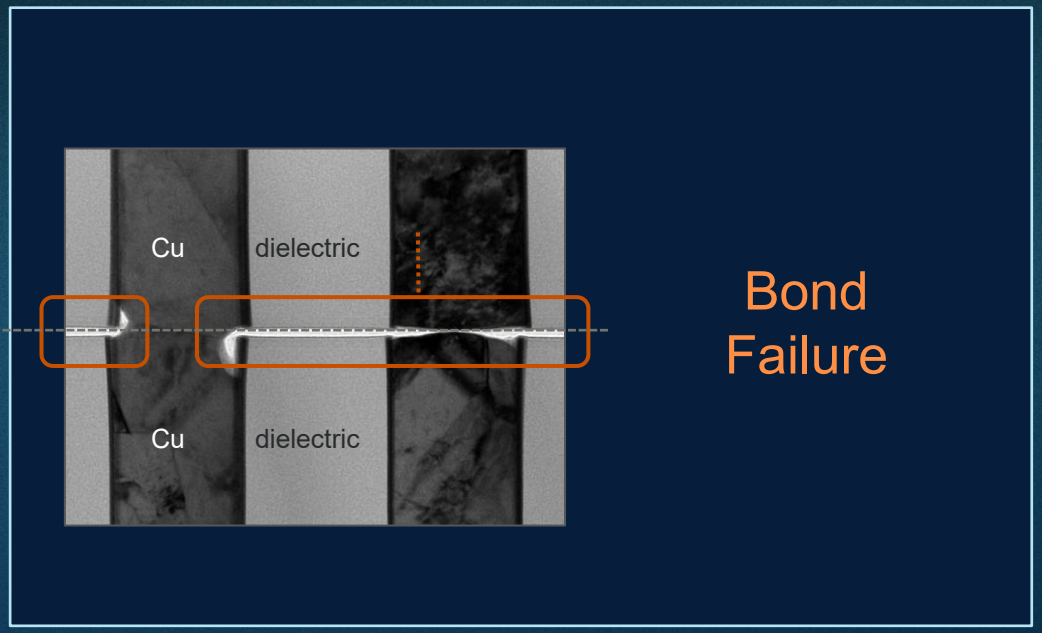
>6.0M Bumps

Source: AMD, MI300X Processor. Applied Materials analysis

Packaging Connections Example: Hybrid-Bonding Challenge







NEED: Dielectric-to-dielectric and copper-to-copper bonding connections without failures

High Technology Complexity Across Front-End and Packaging

Performance, Yield, Productivity (incl. variability control)

Applied's Unique Connectivity Strategy to Solve Complexity

1 Connecting Products, Innovators

Guided by **our unique innovators** with integration and fab production expertise. Materials → Tools → Systems

Innovation

2 Connecting Customers, Partners

Co-development with **Customer R&D leaders**

\+ Connect **partner technologies** on our products

Co-Innovation

3 Connecting Ecosystem in one place

Earlier, deeper, faster collaboration enabled by unique **EPIC R&D center**

High Velocity Co-Innovation

1 Applied's Unique Portfolio: Enables Connecting Technologies

BROADEST CAPABILITIES

	Applied		Competitors			
ALD	✓	✓			✓	✓
Bonding						✓
Cleans					✓	✓
#1 CMP	✓					
#1 CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
#1 Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace						✓
#1 Implant	✓					
Lithography			✓			
M&I (optical)	✓			✓		
#1 M&I (eBeam)	✓		✓	✓		
#1 PVD	✓			✓		
Thermal	✓					✓
Track						✓

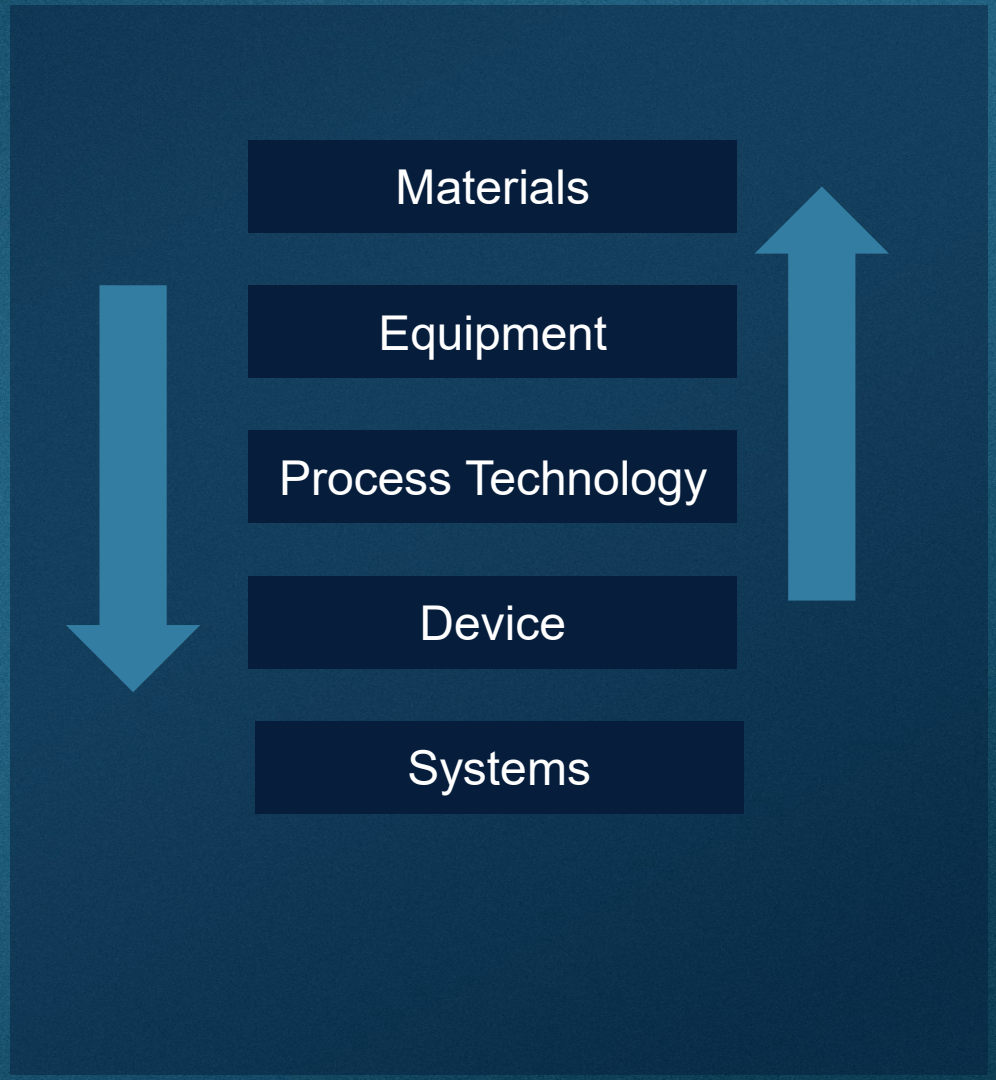
Source for market position ranking: TechInsights

1 Applied's Unique Portfolio: Enables Connecting Technologies

BROADEST CAPABILITIES

	Applied		Competitors			
ALD	✓	✓			✓	✓
Bonding						✓
Cleans					✓	✓
CMP	✓					
CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace						✓
Implant	✓					
Lithography			✓			
M&I (optical)	✓			✓		
M&I (eBeam)	✓		✓	✓		
PVD	✓			✓		
Thermal	✓					✓
Track						✓

UNIQUE INNOVATORS

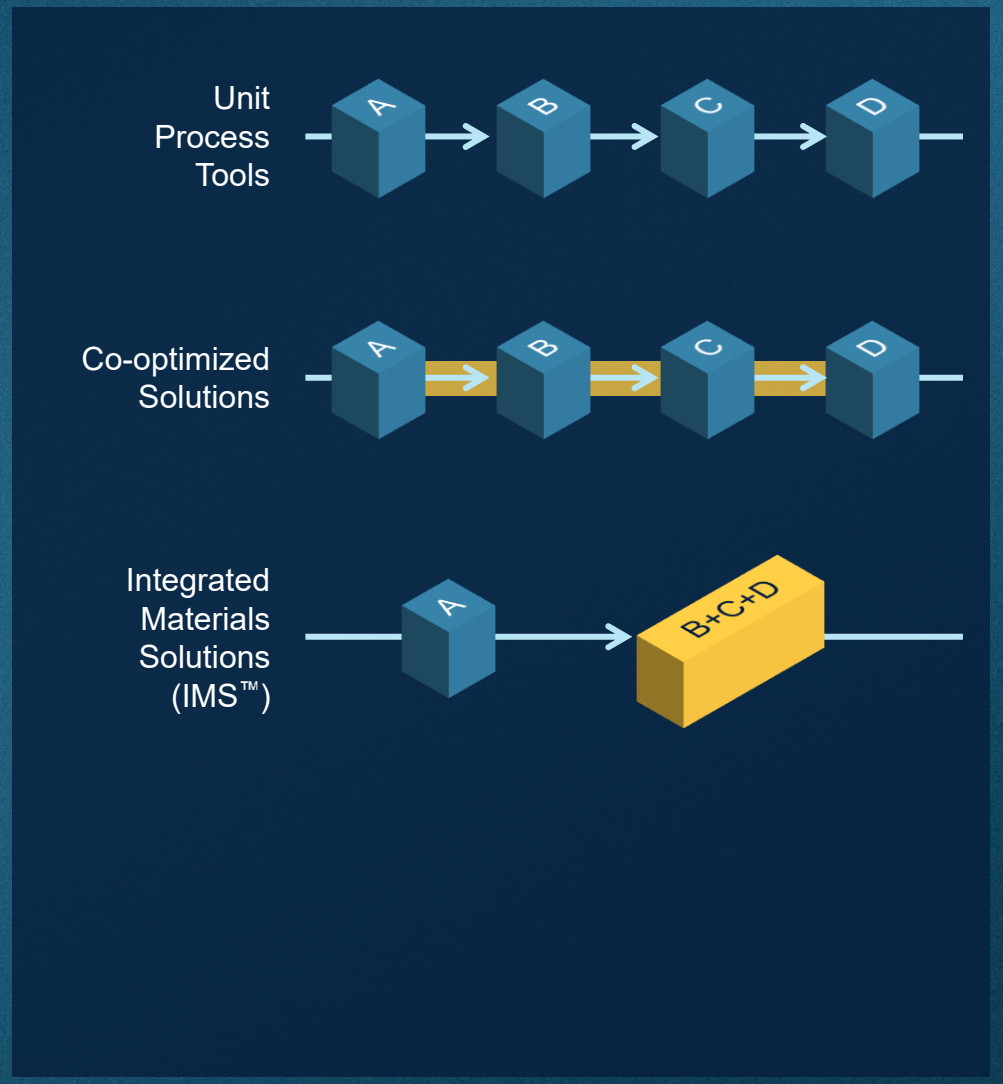


1 Applied's Unique Portfolio: Enables Connecting Technologies

BROADEST CAPABILITIES

	Applied		Competitors			
ALD	✓	✓			✓	✓
Bonding						✓
Cleans					✓	✓
CMP	✓					
CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace						✓
Implant	✓					
Lithography			✓			
M&I (optical)	✓			✓		
M&I (eBeam)	✓		✓	✓		
PVD	✓			✓		
Thermal	✓					✓
Track						✓

UNIQUE COMBINATIONS



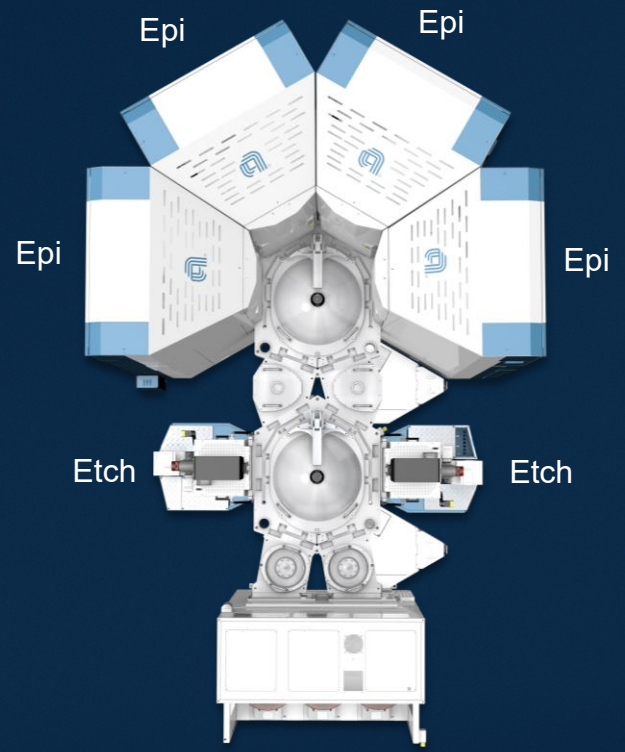
Co-optimization and Integration Improves Resistance, Speed, Power

Co-optimized etch and deposition processes

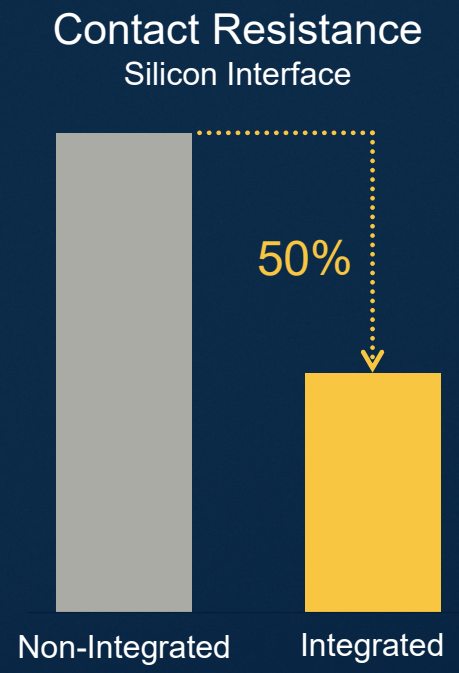
Integrated Materials Solution

Integrated Materials Solution

- Clean
- **Deposition hardmask**
- **Deposition patterning film**
- Track photoresist
- Lithography trench pattern
- Lithography contact pattern
- **Etch patterning film open**
- **Etch hardmask open**
- Etch inter-layer dielectric oxide
- Ash/etch patterning films
- ALD liner deposition
- **Etch source-drain cavity shaping**
- **Epitaxial contact deposition**
- Silicide deposition and anneal
- **Metal cap deposition**
- **Treatment**
- **Metal fill**
- CMP metal overburden removal



Applied Integrated Materials Solution

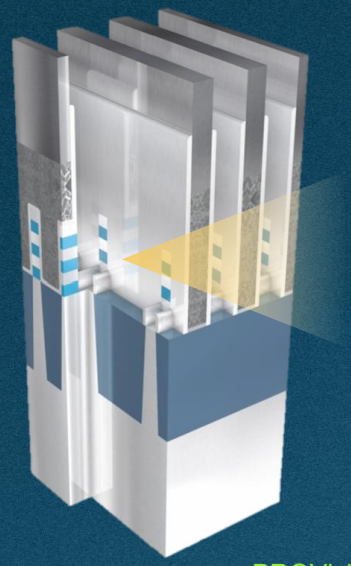


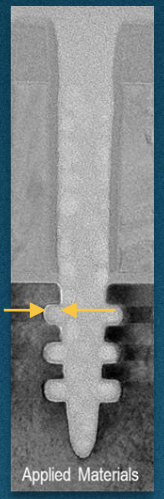
* PMOS DC

50% resistance reduction = Higher performance* (up to 5%↑)

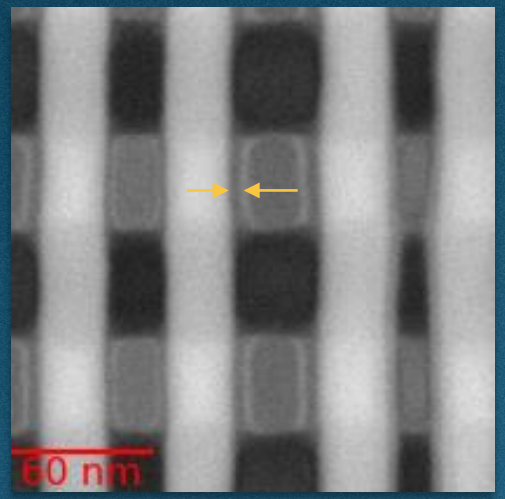
Connecting Process and Metrology → Void-Free Epi Growth

SiGe Recess





Side View



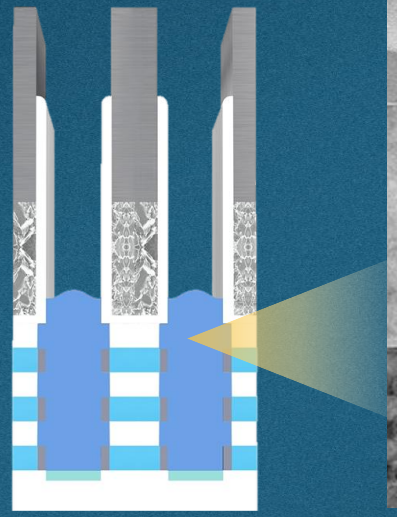
Top View

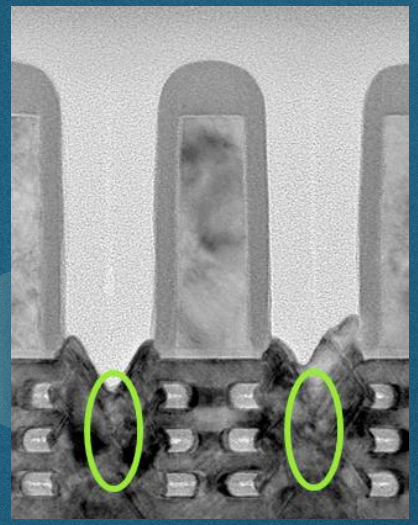
Source: Applied

PROVision™ and Xtera™ co-optimization for void-free uniform growth

Provision metrology for S/D Epitaxy

- Unique capability
- Faster characterization

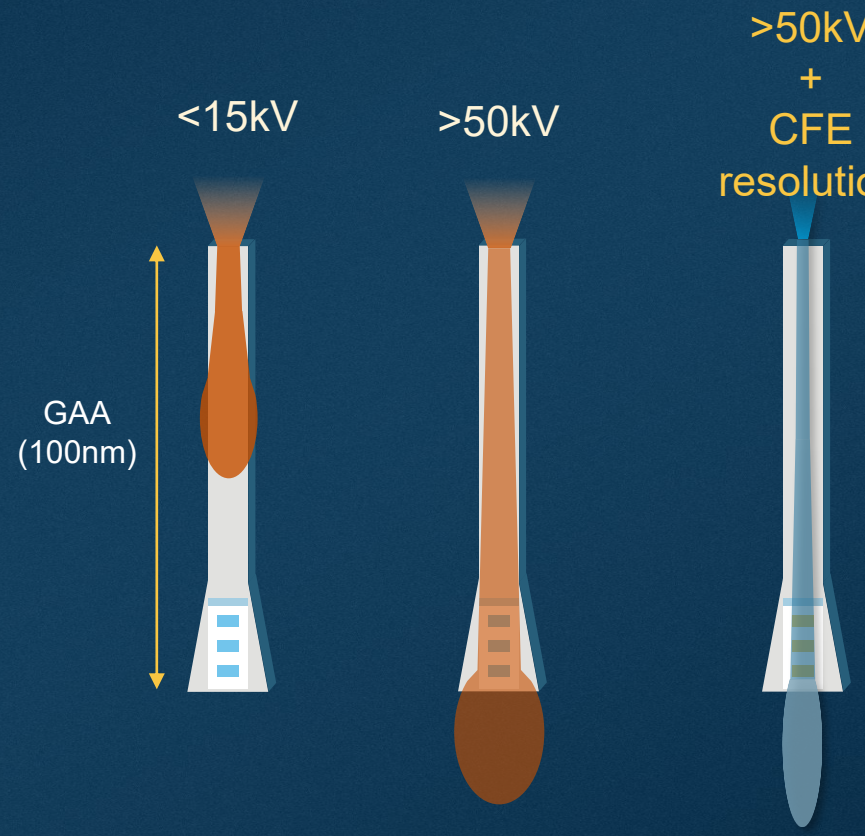




Side View

Source: Applied

PROVision See-Through Imaging



High-resolution imaging through device

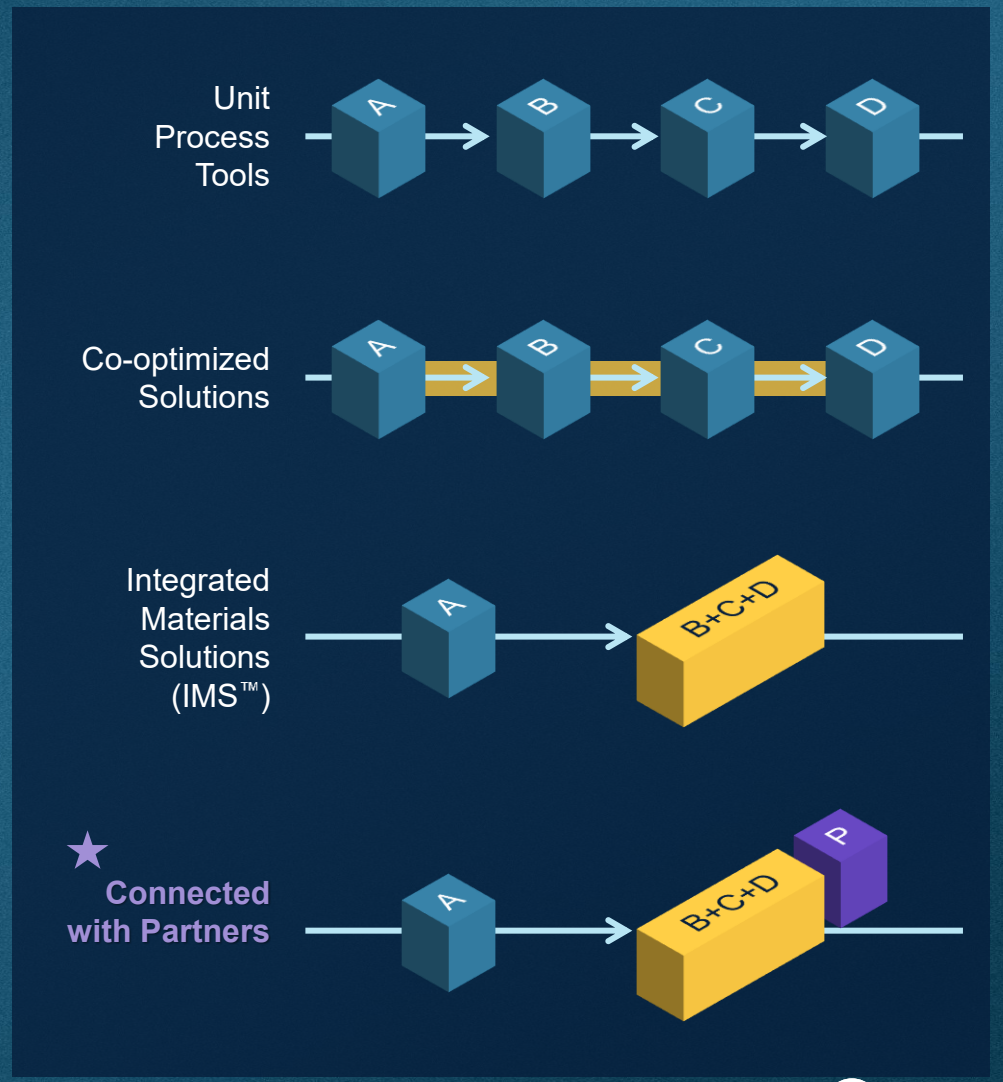
GAA: gate-all-around; SiGe: silicon germanium, CFE: cold field emission

2 Applied's Unique Portfolio: Connecting Partner Technologies

BROADEST CAPABILITIES

	Applied	Competitors				
ALD	✓	✓			✓	✓
Bonding	partner					✓
Cleans	partner				✓	✓
CMP	✓					
CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace	partner					✓
Implant	✓					
Lithography	partner		✓			
M&I (optical)	✓			✓		
M&I (e-beam)	✓		✓	✓		
PVD	✓			✓		
Thermal	✓					✓
Track						✓

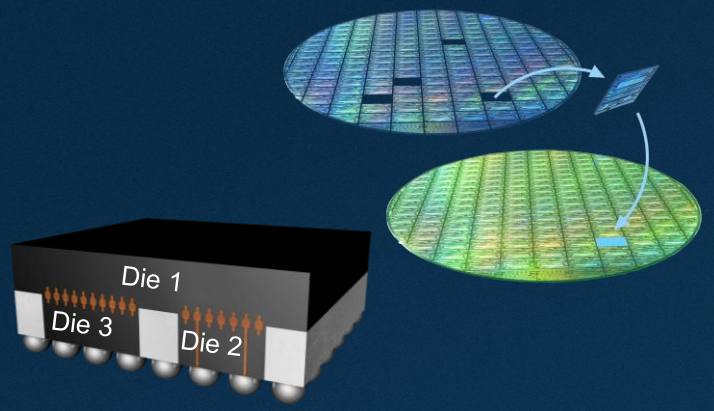
UNIQUE COMBINATIONS



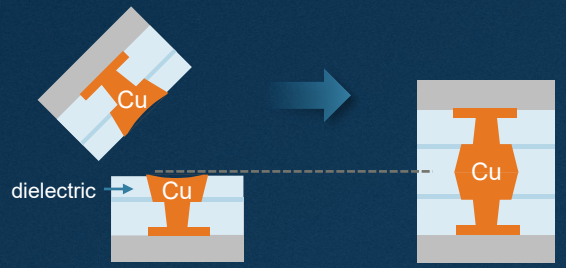
APPLIED MATERIALS

Connecting Partners' Technologies: Co-optimized and Integrated

Die to Wafer Hybrid Bonding



10,000 IO / mm²
≥ 0.1 pJ / bit



Not Optimized

- Bonding CVD
- Pad Etch
- Barrier / Seed
- Cu ECP
- CMP
- Dicing
- Bonding pre-treatment
- Bonding
- Post-bond anneal
- Gap fill CVD
- CMP
- TOV Etch

Co-optimized + Integrated

- Bonding CVD
- Warpage modulation
- Pad Etch
- Barrier / Seed
- Cu ECP
- CMP
- Dicing
- Bonding pre-treatment
- **Bonding**
- Post-bond anneal
- Gap fill CVD
- CMP
- Protective capping
- TOV Etch

Applied + BESI Partnership

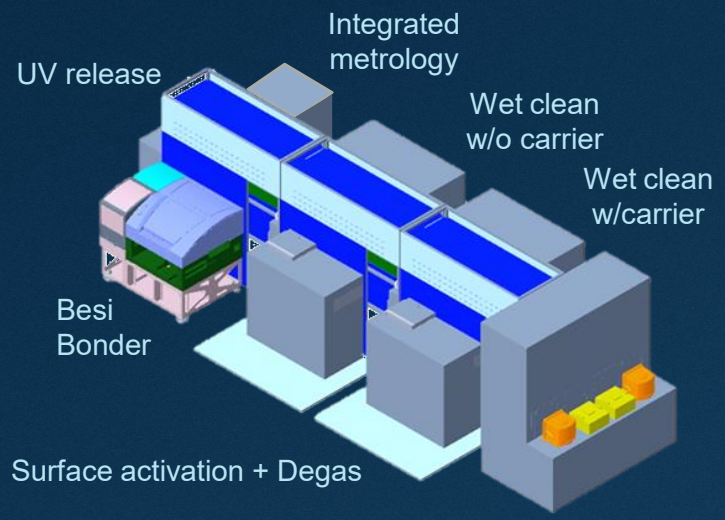
- Wet clean w/ carrier
- Wet clean w/o carrier
- Plasma activation
- UV release
- **Bonding**
- Metrology

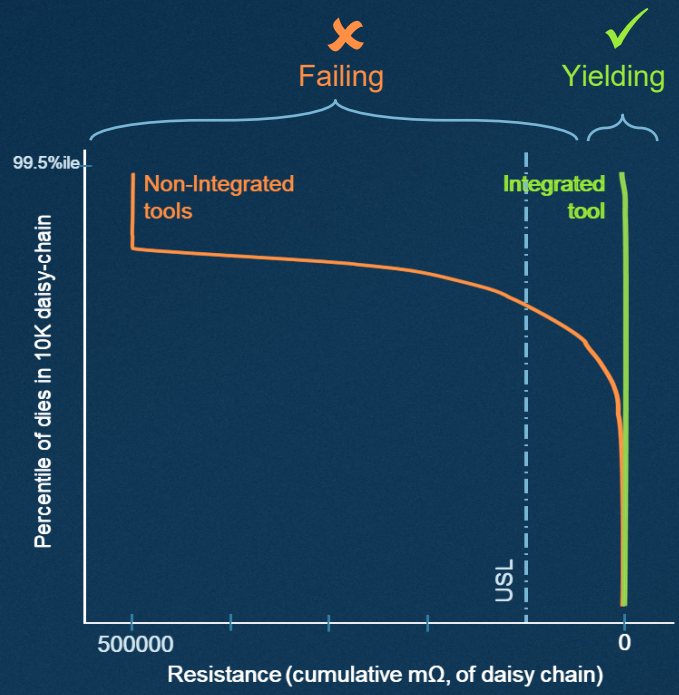
Co-optimized Processes

Integrated Processes

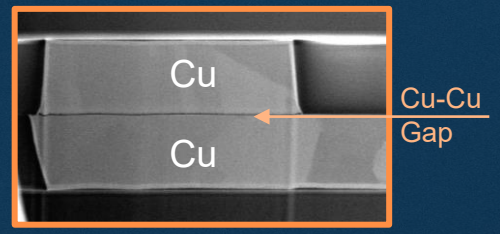
Value of Joint Integrated Processes: Bond Strength and Yield

6 steps all integrated in one tool → Mitigating **queue-time** for higher yield

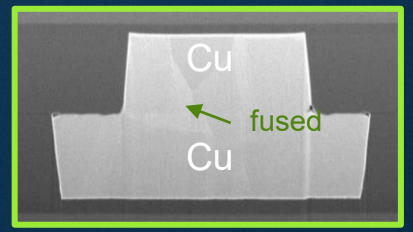




✘ Contamination risk
✘ Queue time issues

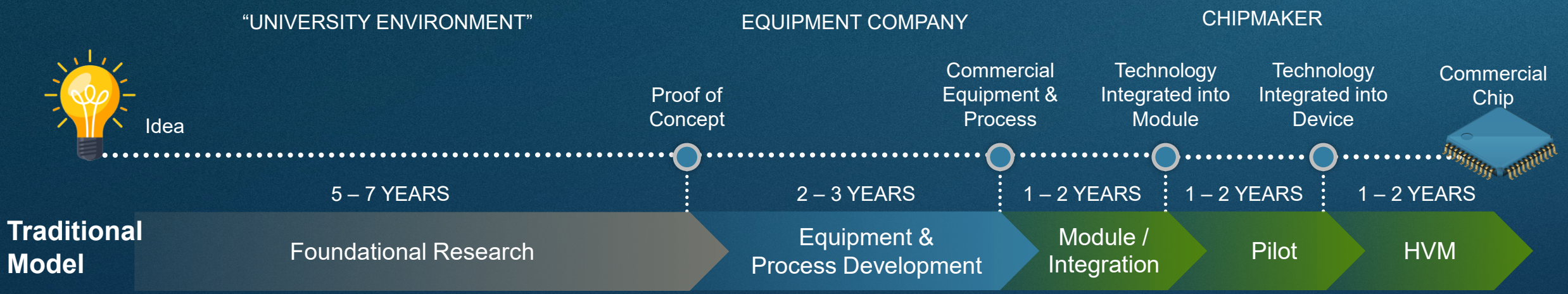


✓ Improved adhesion
✓ Improved yield



Kinex™ Integrated Die-to-Wafer Hybrid Bonding System

3 Complexity: Slow Innovation-to-Commercialization Cycle

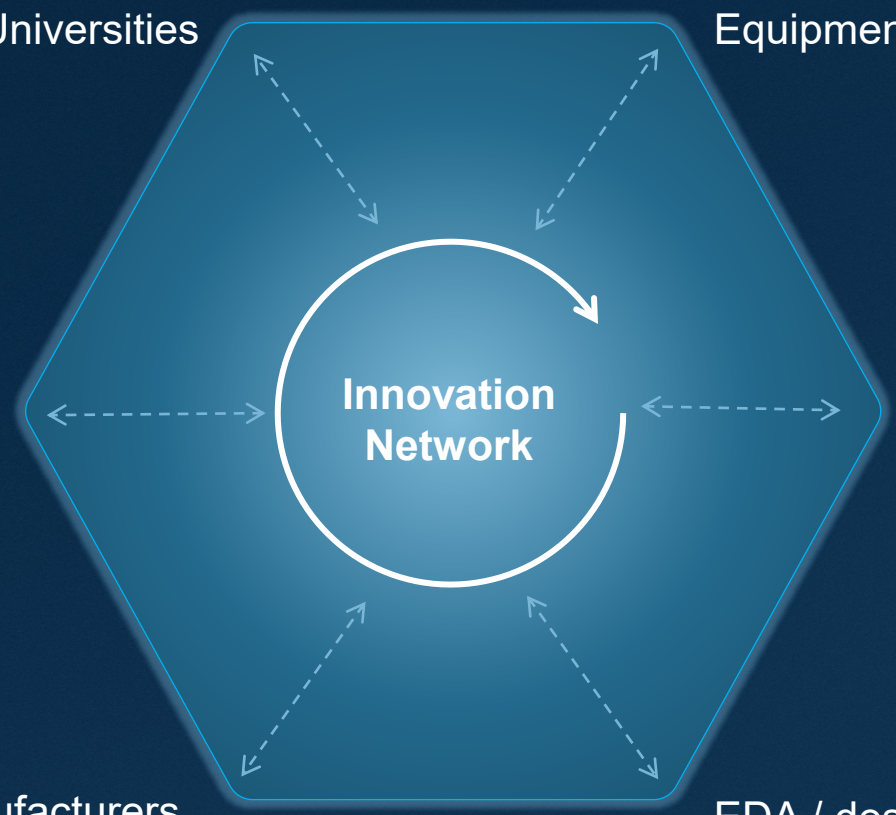


Can Take **10-15 YEARS** Today!

2023

3

Connecting Ecosystem + Connecting Them in One Place



+

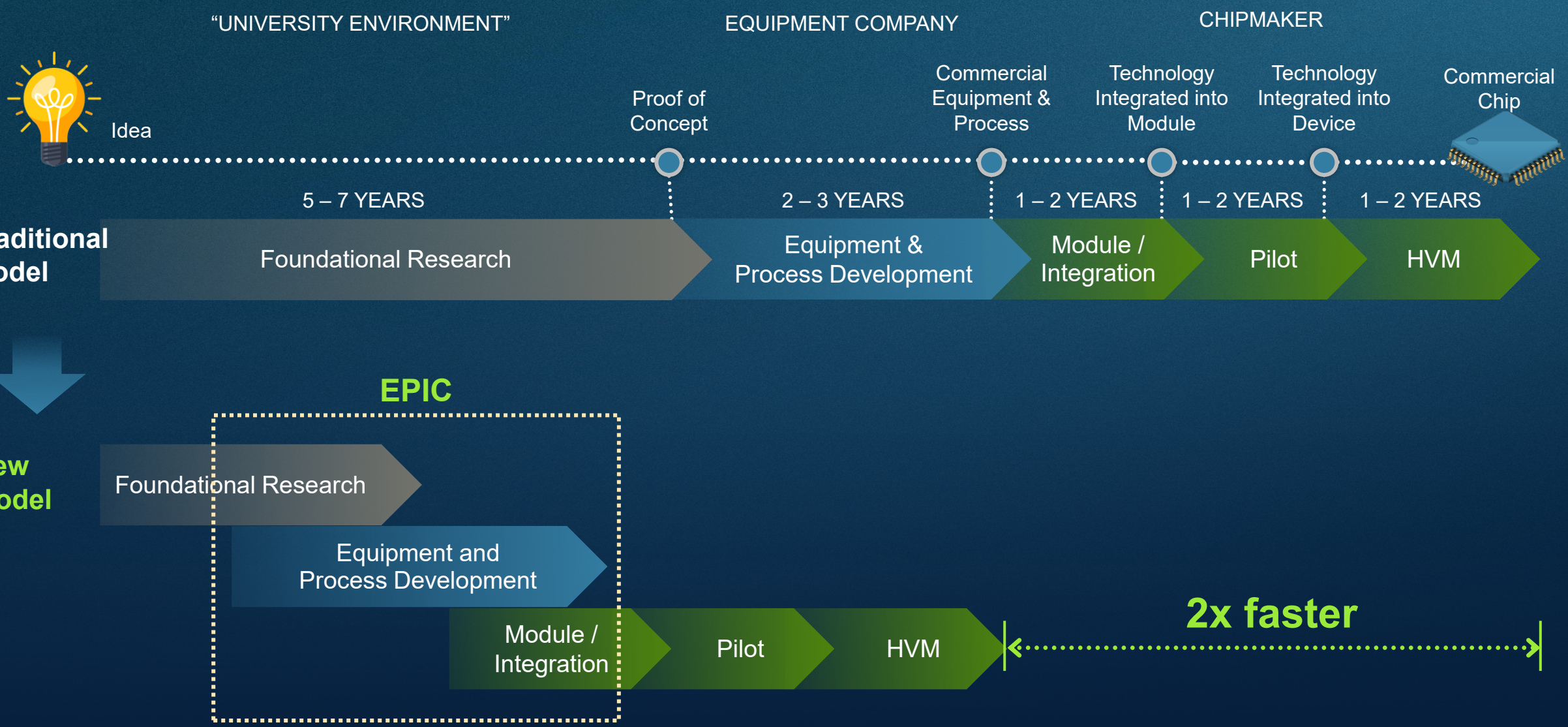
New R&D Center Opening 2026

EPIC CENTER

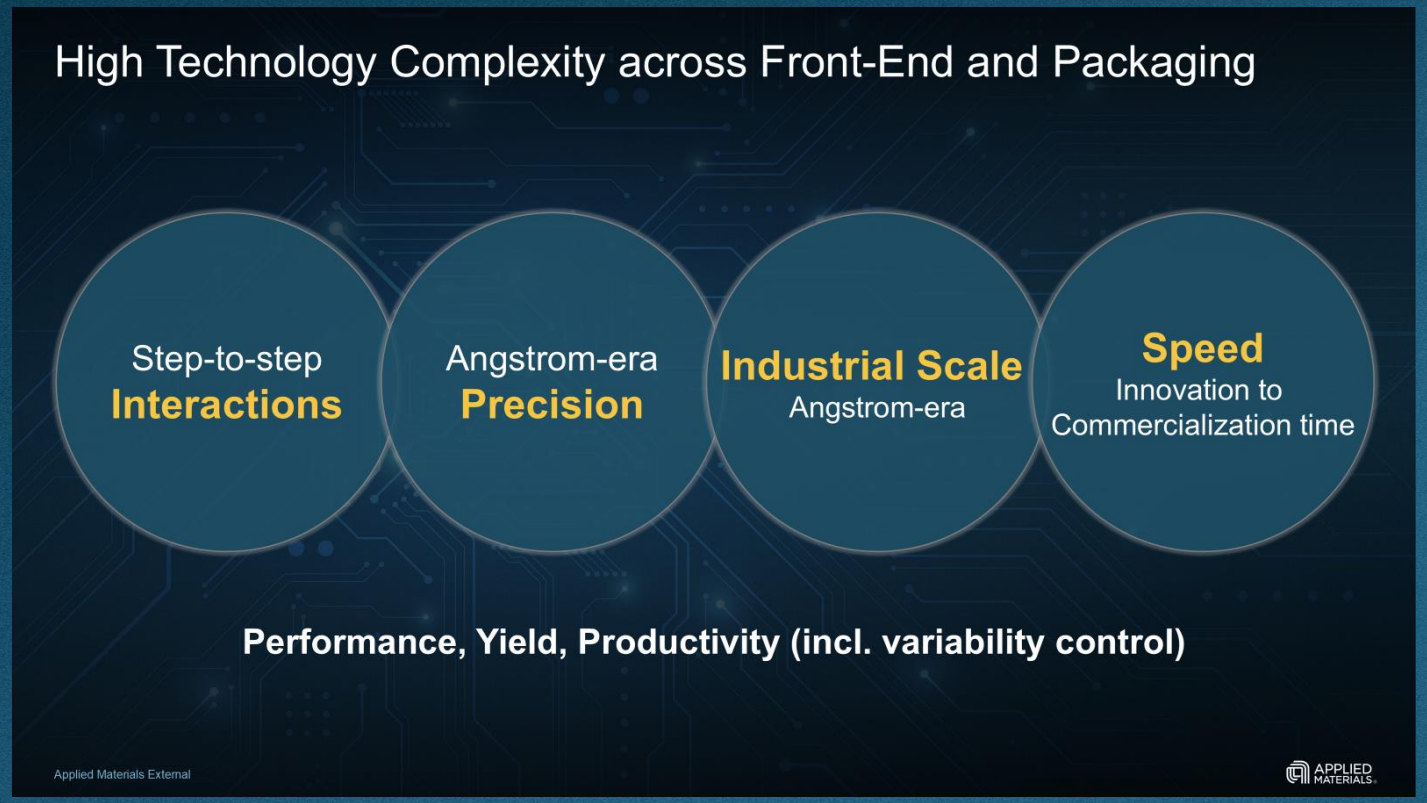
First access to new materials innovations (years before anyplace else)

Highest velocity co-innovation – critical to win the race for new chip architectures

EPIC Center Will Enable Faster Innovation and Commercialization



Complexity Recap



Solving Complexity

1. Connecting
   Products, Innovators
2. Connecting
   Customers, Partners
3. Connecting
   Ecosystem in one place

Product Launch

New Products Seeing Strong Customer Adoption

Applied Centura™ Xtera™ Epi

Enables void-free fill at ≤2nm nodes
Unique, smallest-volume epi reactor

PROVision™10 eBeam Metrology

On-device 0.95nm see-through resolution
World's first metrology-grade CFE System

Kinex™ Integrated Die-to-Wafer Hybrid Bonding System

10-20X ↓ queue time ↑ bond quality, ↑ yield
Revolutionary mini-environment:
materials processing + bonding + metrology

APPLIED MATERIALS

Enablement

Mukund Srinivasan, Ph.D.

Vice President and General Manager, Semiconductor Products Group

OCTOBER 7, 2025

Recap on Enabling AI Everywhere

Jim Chambers
Vice President, NVIDIA

AI is the fifth industrial revolution, transforming every industry

AI's demand drives nonstop innovation in silicon, packaging, and architecture

Deep ecosystem collaboration is essential for unlocking the next wave of AI growth

Rose Castanares
President, TSMC Arizona

AI is everywhere, and its growth is driving exponential power demand

Advanced logic and 3D packaging are essential for energy-efficient AI

Industry-wide collaboration is the only way to meet AI's challenges at global scale

Semiconductor Devices are Enabling AI

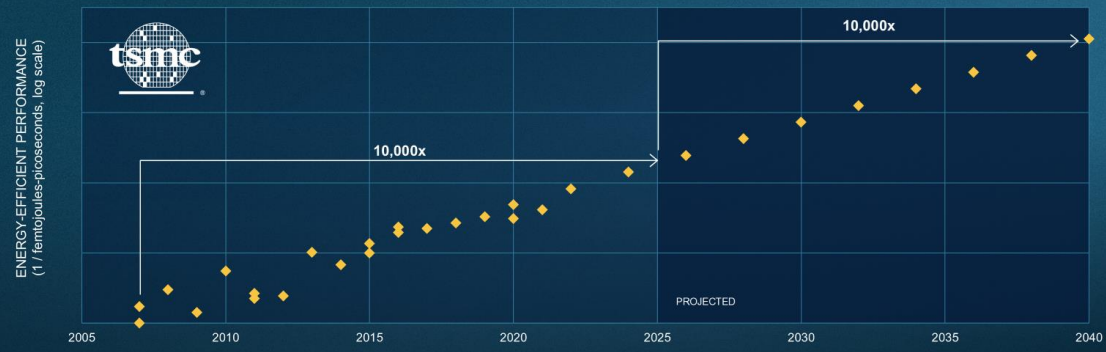
Semi Devices Foundational for Energy Efficient Performance

- Leading-edge Logic
- High-performance DRAM
- High-bandwidth DRAM
- Advanced Packaging
- Power semi (ICAPS)

ICAPS: Internet of Things, Communications, Automotive, Power and Sensors

Improvements are Needed for Energy Efficiency

10,000x Improvement Needed in Next 15 Years



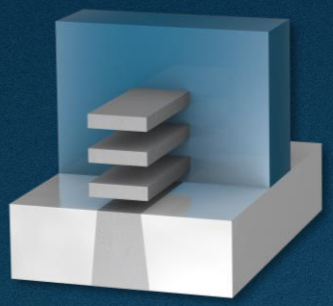
Global Race for AI Leadership Determined by Energy-Efficient Computing Performance

Source: Mark Liu and H.-S. Philip Wong, IEEE Spectrum, March 28, 2024. https://spectrum.ieee.org/trillion-transistor-gpu

The Industry Must Deliver:
More Compute, More Bandwidth, Less Energy – Faster

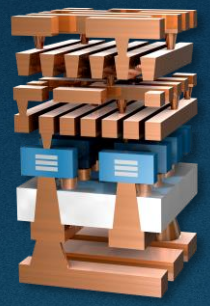
3D Architecture Inflections Will Unlock AI Potential

AI Leading-edge Logic



GAA Transistor

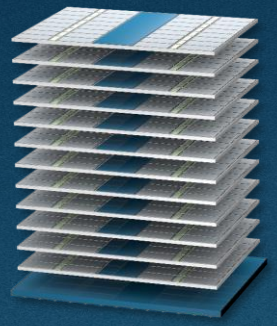
30% ↓ power,
15% ↑ performance



Backside Power

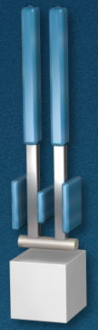
30% ↑ density
↑ 10% performance

AI DRAM: HBM + Leading Edge



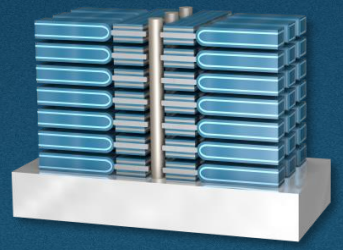
High Bandwidth Memory

Bandwidth +1,000%



Vertical Transistor

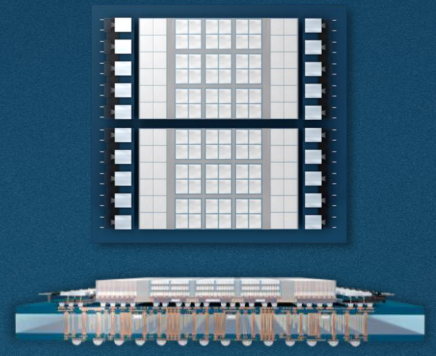
EEP +15%



3D DRAM

EEP +15%

AI Sys. Integration



Advanced Packaging

1000x ↑ IO / mm²
10x lower pJ / bit ↓

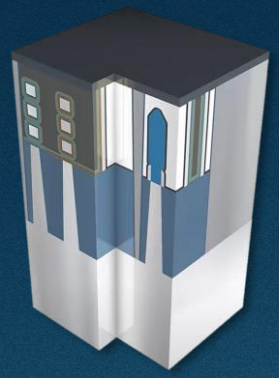
Enabled by new materials, selective deposition and removal, and process step interactions

IO: input/output, EEP: energy-efficient performance

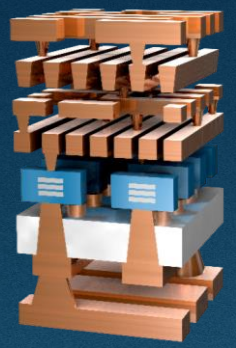
Priorities for Next-Generation AI Device Enablement

SILICON ENABLEMENT

LOGIC

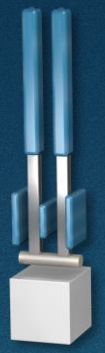


Transistor Scaling



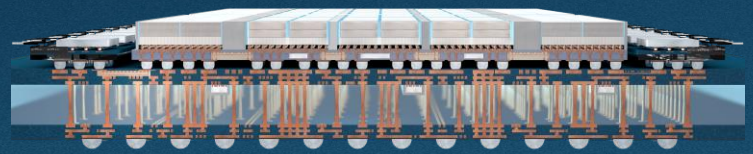
Interconnect Scaling

DRAM



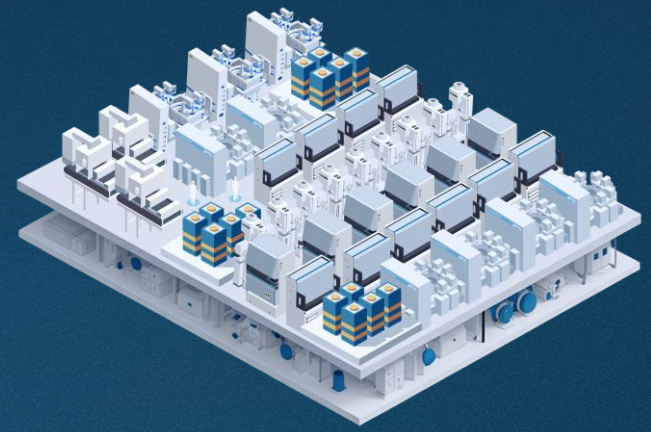
$4F^2$ VT

PACKAGE ENABLEMENT



2.5D and 3D Integration

FAB ENABLEMENT



R&D and Ramp Acceleration

Enablement Expert Panel

SILICON ENABLEMENT

Bala Haran, Ph.D.

Vice President
Integrated Materials Solutions
Semiconductor Products Group

PACKAGE ENABLEMENT

Subi Kengeri

Vice President
General Manager
Systems to Materials

FAB ENABLEMENT

Mike Chudzik, Ph.D.

Vice President
Technology
Semiconductor Products Group

Steve Frezon

Vice President
Customer Services & Support
Applied Global Services

Silicon Enablement

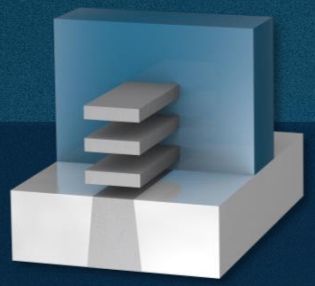
Bala Haran, Ph.D.

Vice President, Integrated Materials Solutions, Semiconductor Products Group

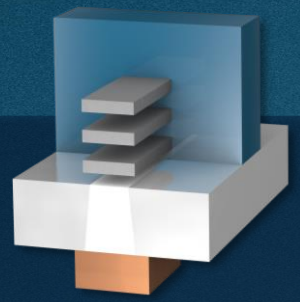
OCTOBER 7, 2025

Silicon Enablement Roadmap

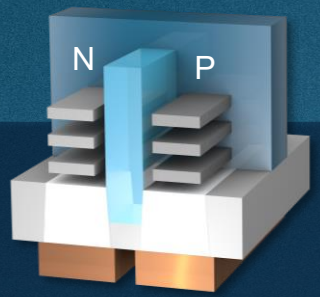
LOGIC



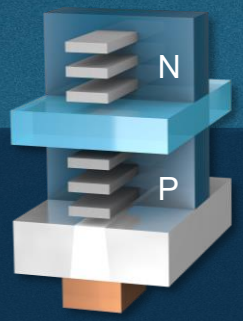
GAA



GAA with Backside Power



GAA with Isolation



CFET

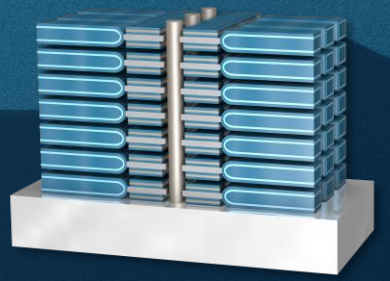
GAA: gate-all-around
CFET: complementary field effect transistor

DRAM

$8F^2$ RCAT

$6F^2$ BCAT

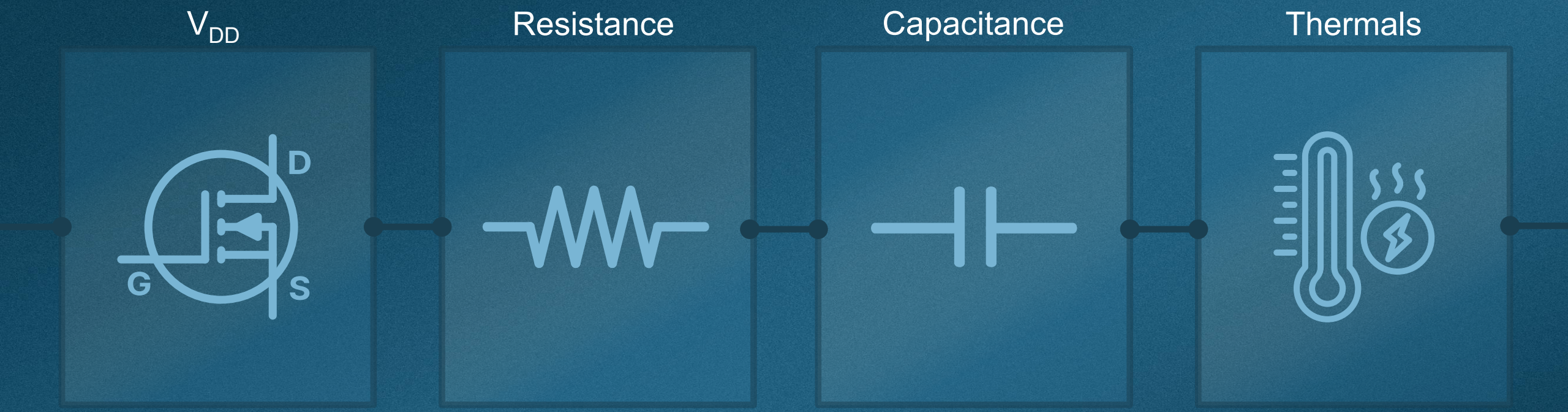
$4F^2$ VT



3D DRAM

RCAT: recessed channel array transistor
BCAT: buried channel array transistor
VT: vertical transistor

Key Levers for Energy Efficient Compute



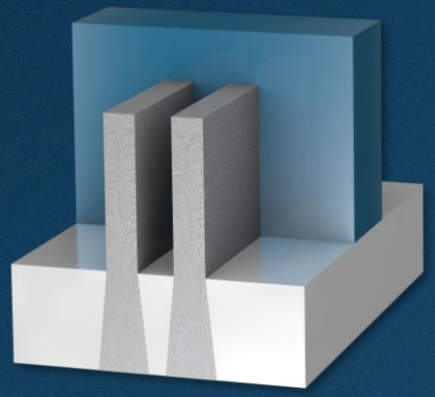
$$P_{dynamic} = \alpha C V_{DD}^2 f$$

$P_{dynamic}$: power consumed to perform operations
α : activity factor
C : capacitance

V_{DD} : supply voltage
f : clock frequency

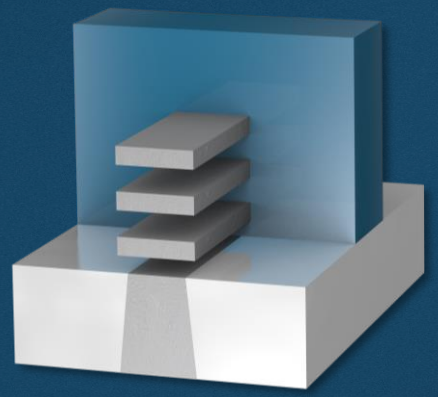
Voltage Reduction with GAA

800 mV
700 mV
600 mV
500 mV
400 mV



FinFET

150 mV
Lower V_{DD}



GAA

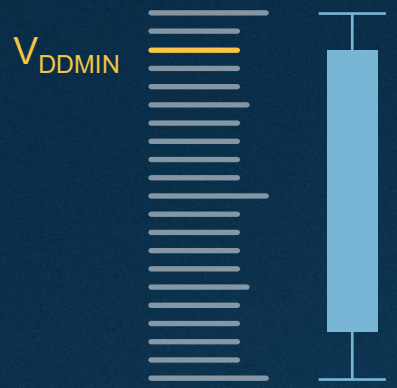
⬇30%
Dynamic Power

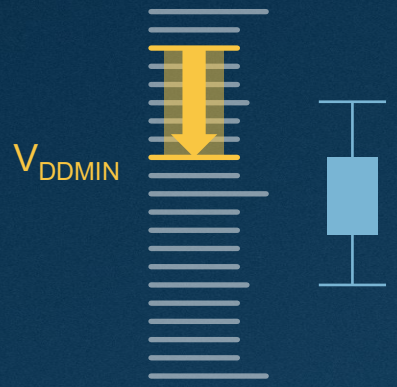
Applied Materials enables >50% of the process steps required for GAA

FinFET : fin field effect transistor
GAA: gate-all-around

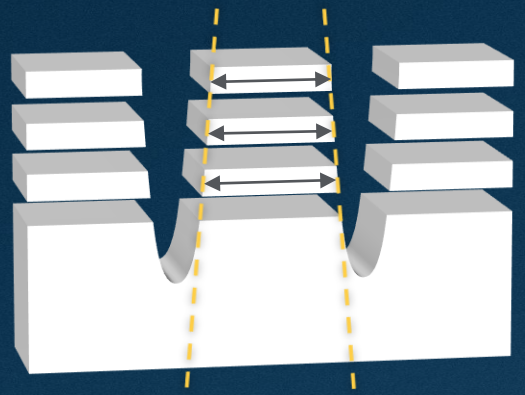
Voltage Variability Reduction

V_{DD} Variability

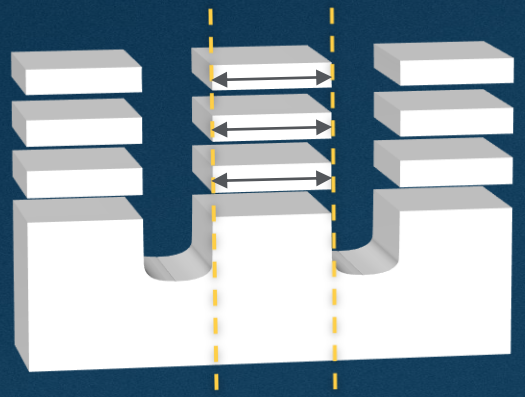




Etch Profile Control

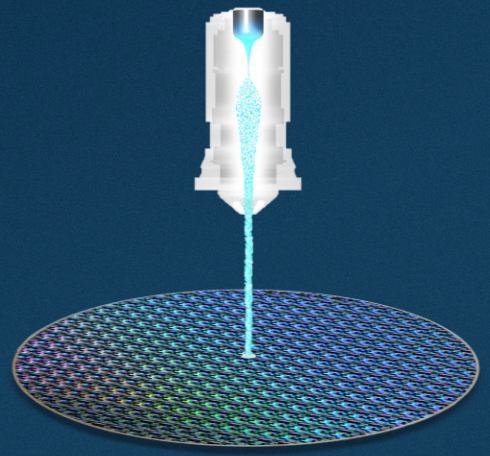


Variable gate lengths



Uniform gate lengths

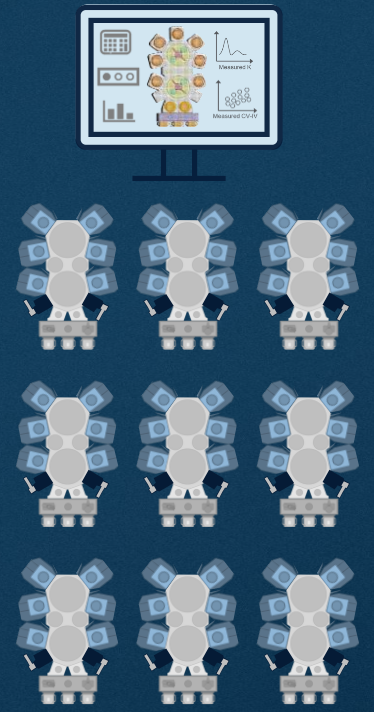
Metrology Monitoring



Massive measurements across entire wafer

Top-to-bottom CD variation translates to gate and channel length variation

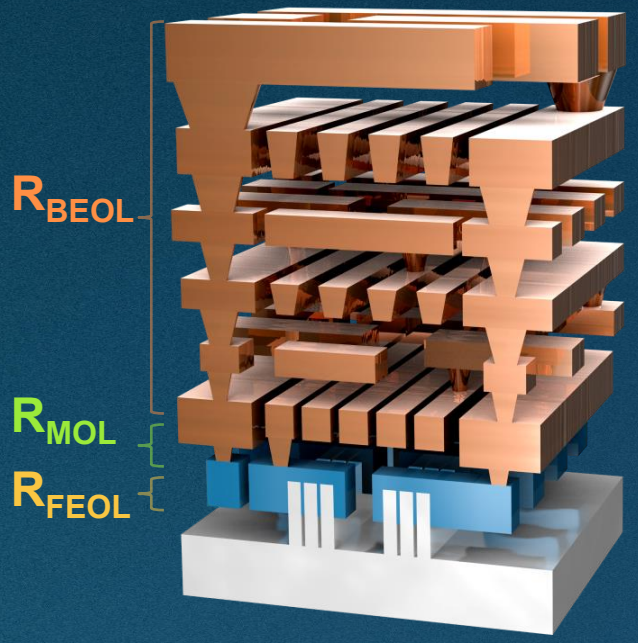
AI^X Monitoring



Wafer-level to fleet-level variation control

Sym3™ Z Etch ✚ PROVision™ 10 eBeam Metrology ✚ AI^X™ Platform

Co-optimized process control critical to minimize variability

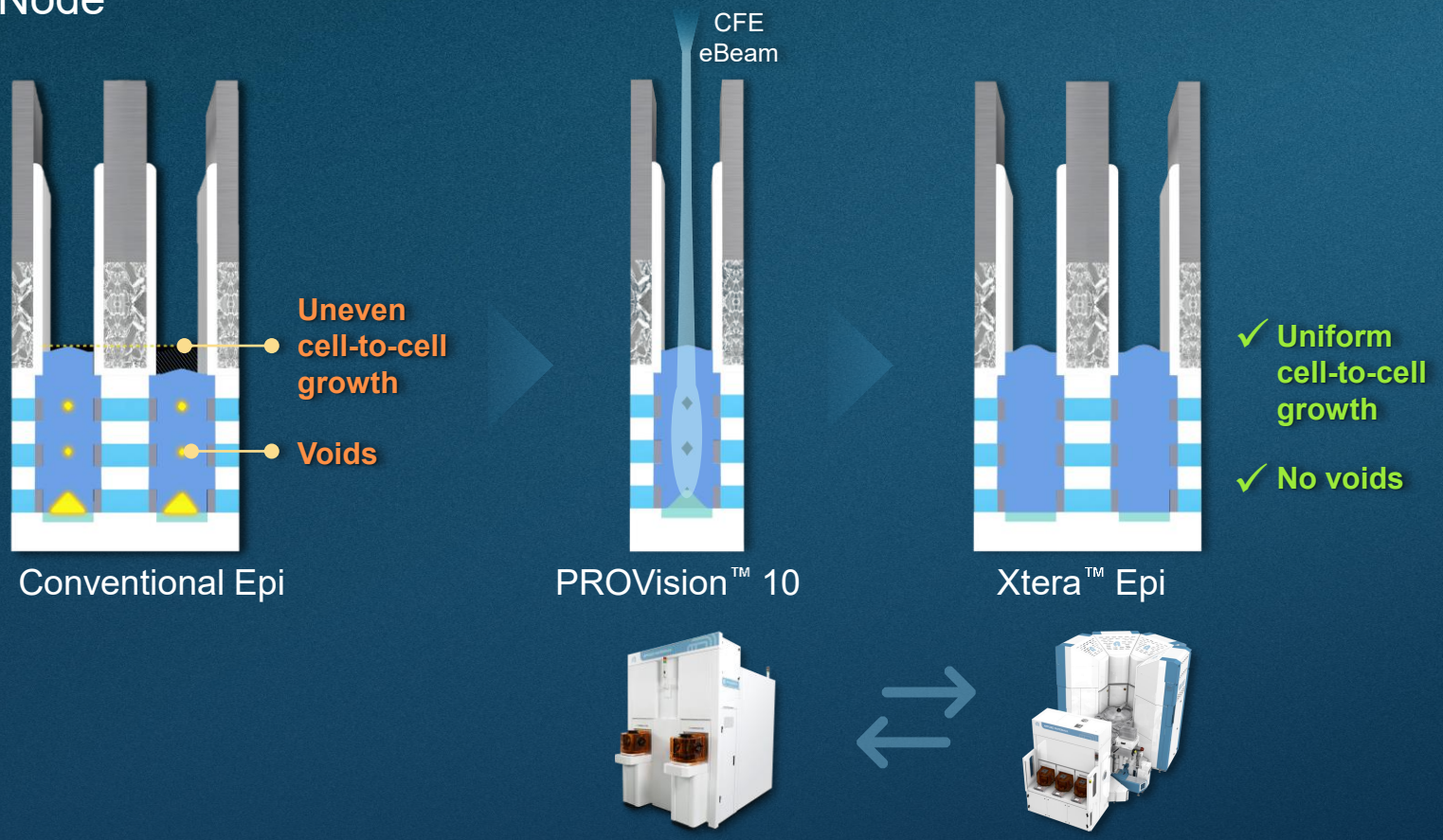


$$Resistance_{TOTAL} = R_{FEOL} + R_{MOL} + R_{BEOL}$$

FEOL: Front End of Line (Transistor)
MOL: Middle End of Line (Contact & Local Interconnect)
BEOL: Back End of Line (Interconnect Wiring)

Resistance FEOL | Precision Epitaxy and Massive Metrology

GAA S/D Epi @ ≤ 2nm Node



Uniform void-free epitaxy co-optimized using fast scalable metrology

CFE : cold field emission
GAA: gate-all-around
S/D: source / drain

Resistance MOL | Integrated Solutions to Lower Resistance

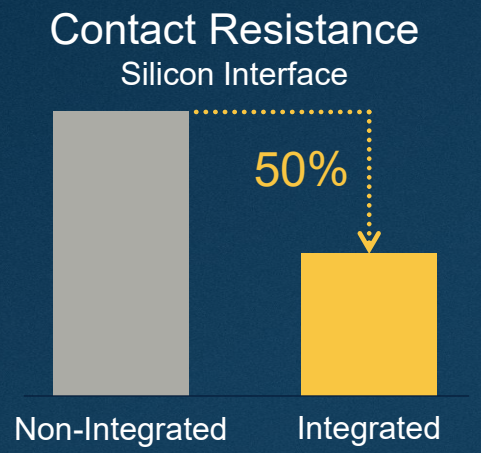
GAA Contact Junction

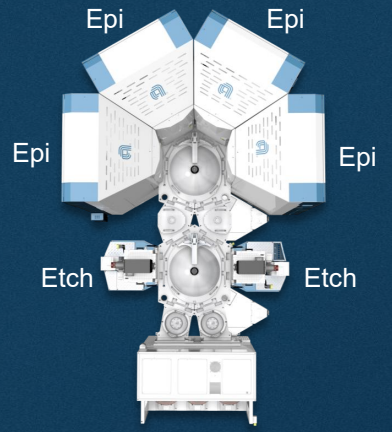
Co-optimized etch and deposition processes

Integrated Materials Solution

Integrated Materials Solution

- Clean
- **Deposition hardmask**
- **Deposition patterning film**
- Track photoresist
- Lithography trench pattern
- Lithography contact pattern
- **Etch patterning film open**
- **Etch hardmask open**
- Etch inter-layer dielectric oxide
- Ash/etch patterning films
- ALD liner deposition
- **Etch source-drain cavity shaping**
- **Epitaxial contact deposition**
- Silicide deposition and anneal
- **Metal cap deposition**
- **Treatment**
- **Metal fill**
- CMP metal overburden removal

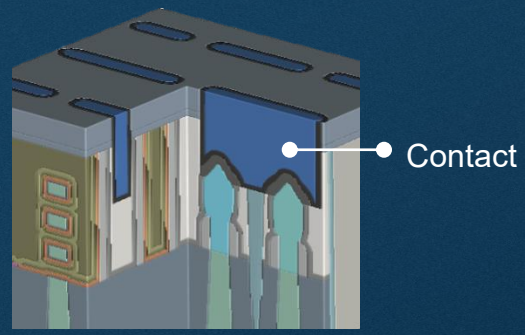


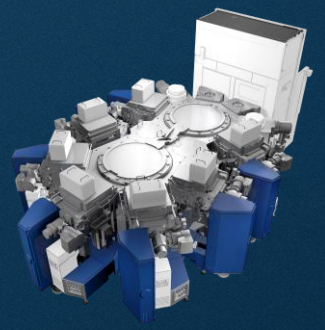


Applied Integrated Materials Solution

GAA Contact Metal

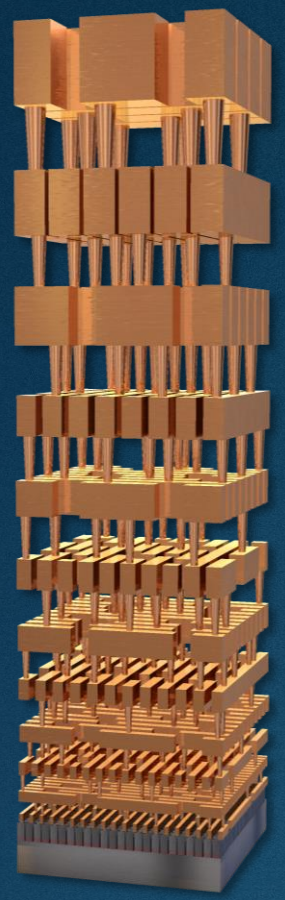
Node	Contact
~7 nm:	Liner with Cobalt
2 nm:	Selective Tungsten
<2 nm:	Selective Moly





Applied Endura™ Integrated Materials Solution

Resistance BEOL | Reclaiming Conductivity for AI Performance



Interconnects

>750 miles of wiring in an AI GPU processor

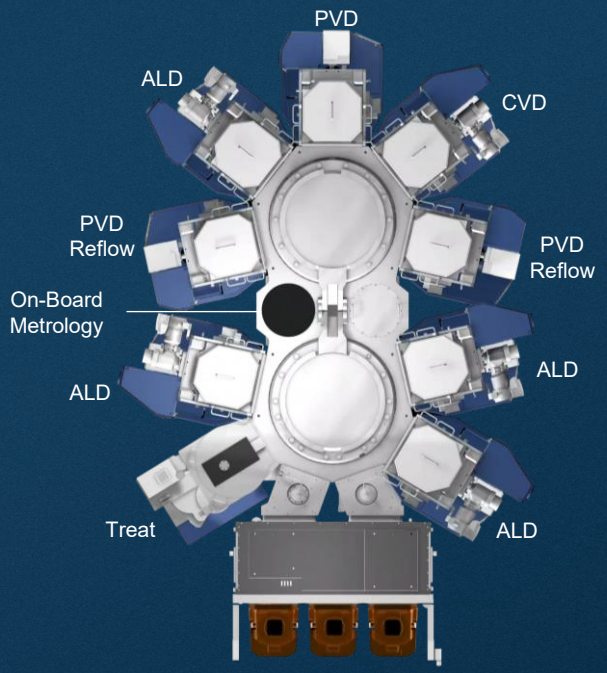
>20 layers stacked copper

>15 stacked layers of Low-κ films

>80 billion transistors

End-to-End Metals Co-optimization

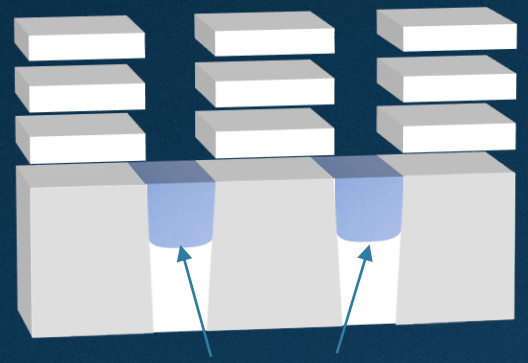
Selective Liners/Barriers	Endura™ IMS
Seam/Void-free Gapfill	Endura™ PVD
Advanced Treatment	Pyra™ Anneal
Advanced CMP	Opta™ CMP



7 Steps in Vacuum Unique to Applied

Capacitance | Engineered with Advanced Materials and Processes

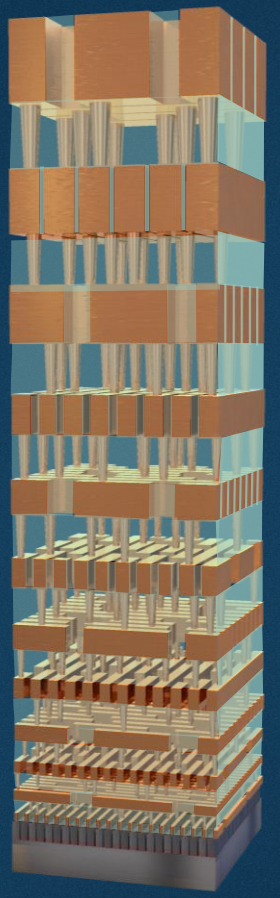
FEOL



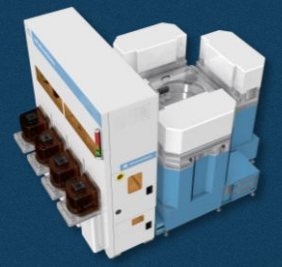
Bottom Dielectric Isolation (BDI)

Co-optimized
CVD + Advanced Treatment + Etch

BEOL



Low-κ Dielectric



Enhanced
Black Diamond™
Low-κ Dielectric Film

+

Opta™ CMP

Connected Technologies Lower Capacitance to Cut Dynamic Power Losses

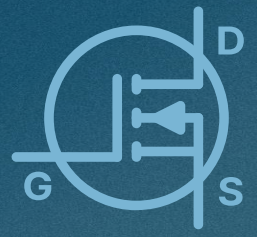
Thermal Management Key in 3D Integrated Circuits

PREVENTION

Excessive heat degrades chip performance (frequency, I_{on})

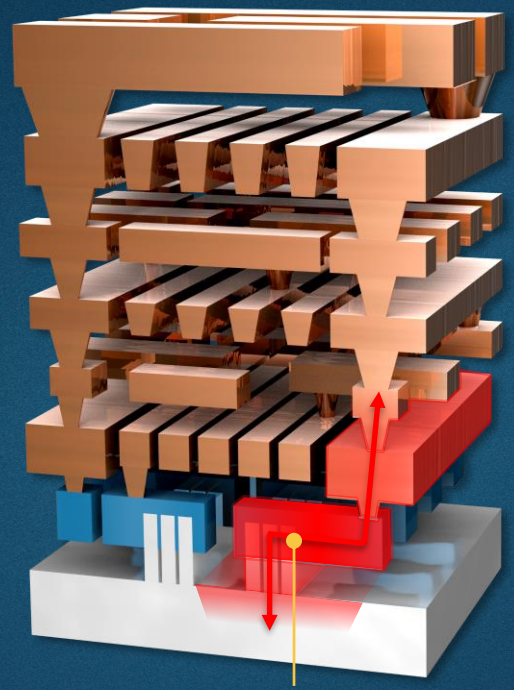
MANAGEMENT

Low V_{DD}



Low R

Low C



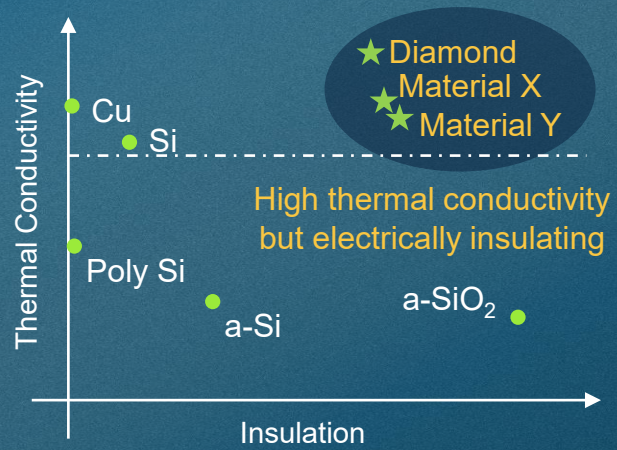
+10°C to +15°C hot spot

System-Level Solutions

Co-design removal paths

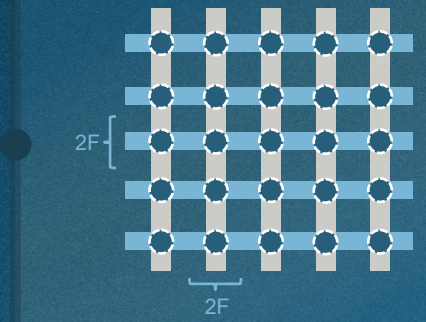
New Materials

Improved thermal conduction



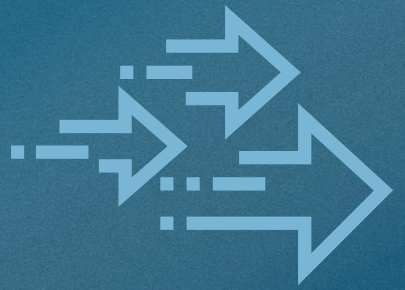
Memory | Key Levers for Energy Efficient Compute

Capacity



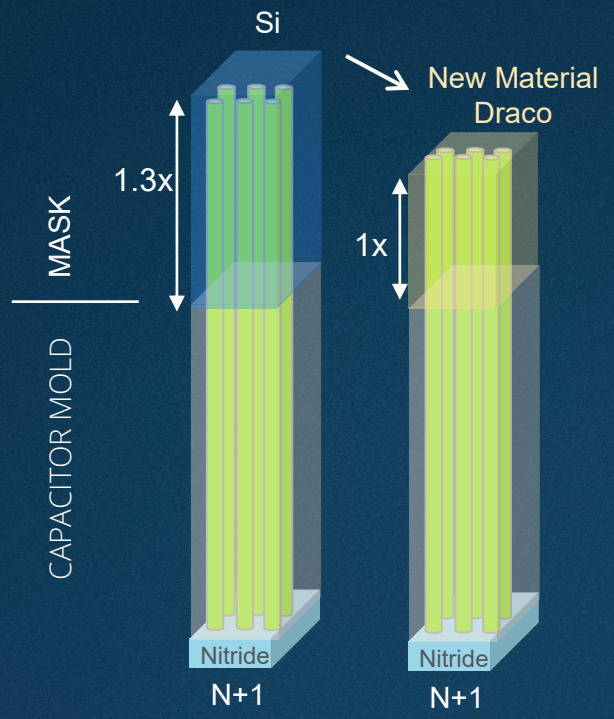
Bandwidth

Speed



Materials Etch and Metrology Innovations Enable Capacitor Scaling

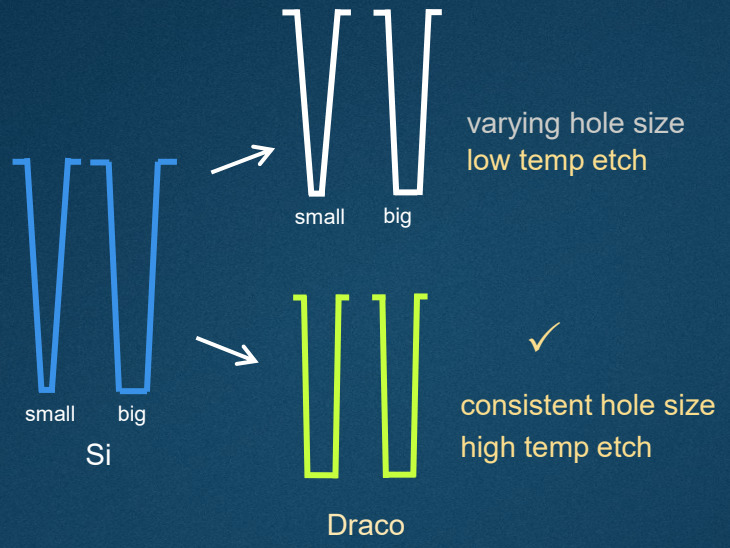
Draco™: New hard mask material
(Higher modulus and selectivity)



Tunable film properties for selectivity
Unique precursor chemistry

+

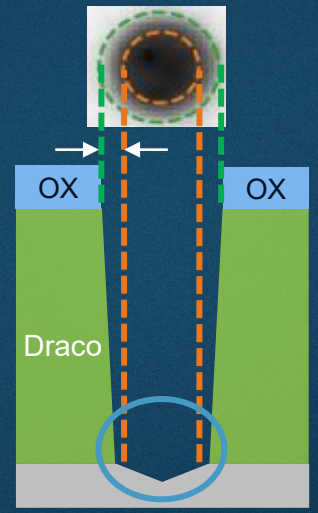
New high temp etch technology
(Better profile and CD uniformity)



Industry leading >200°C capability
Higher conductance Sym3™ design

+

Unique metrology
(Faster and better sampling error)

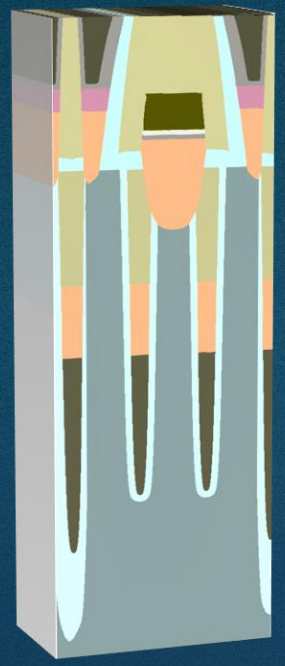


Non-destructive, bottom imaging with actionable measurements

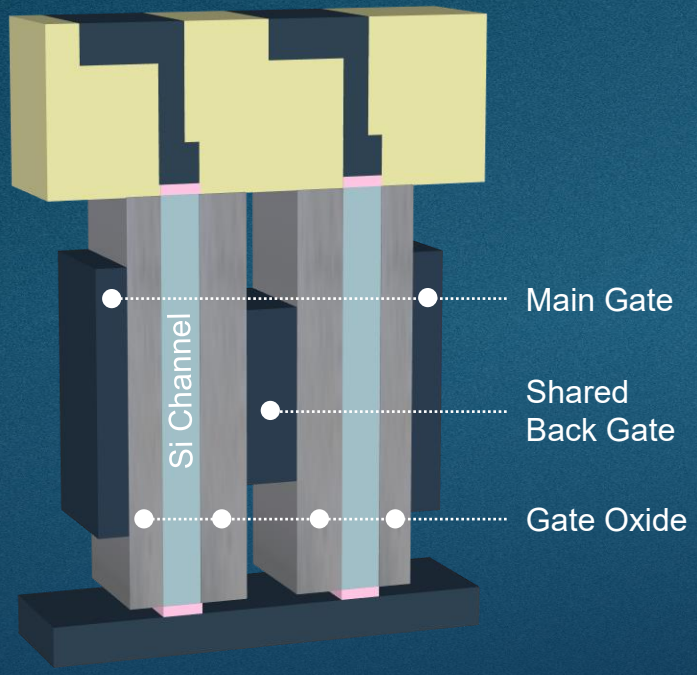
* CD = Critical Dimension

Architectural Innovation to Scale DRAM Density

$6F^2$
BCAT Transistor



$4F^2$
Vertical Transistor

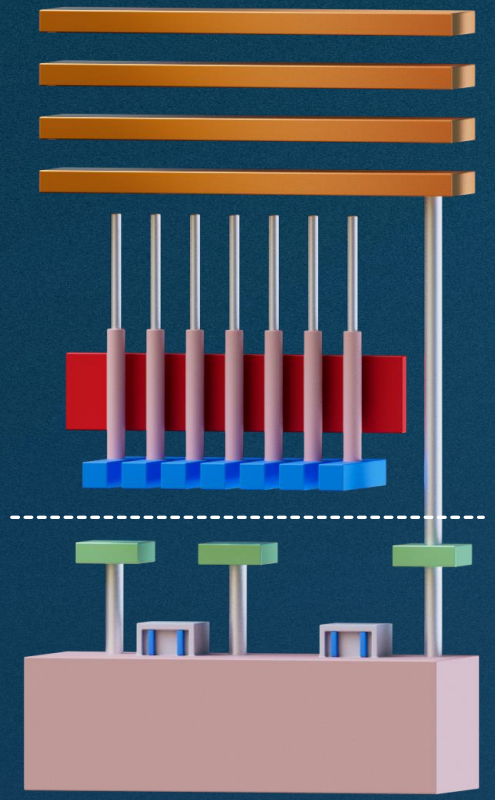


Challenge	Solution
High aspect ratio vertical channel profiles	Sym3 Z Etch
Interface traps	Centura RPO + RTH

RPO: remote plasma oxidation, RTH: rapid thermal processing with H_2

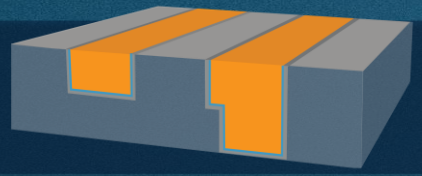
Applied's broad portfolio in etch, deposition & treatments critical for DRAM scaling

DRAM Speed & Performance



Interconnect

Black Diamond™ Low-k
Cobalt Seed Enhancement
Cobalt Cap

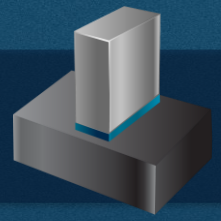


Cu Interconnect

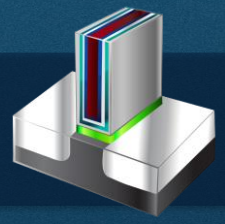
Advanced ULK Cu Interconnects

Transistor

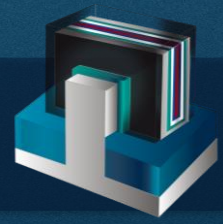
Celera™ SiN PECVD
eSiGe
Stress Films



Poly Gate Transistor



HKMG w/ Embedded SiGe



FinFET

Applied's leading innovations in logic being Adopted in memory

Package Enablement

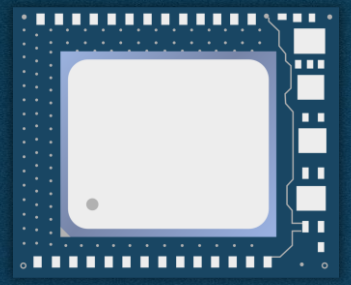
Subi Kengeri

Vice President and General Manger, Systems to Materials

OCTOBER 7, 2025

Packaging Complexity in the AI Era

STATE-OF-THE-ART
Server Processor



PCF: 1

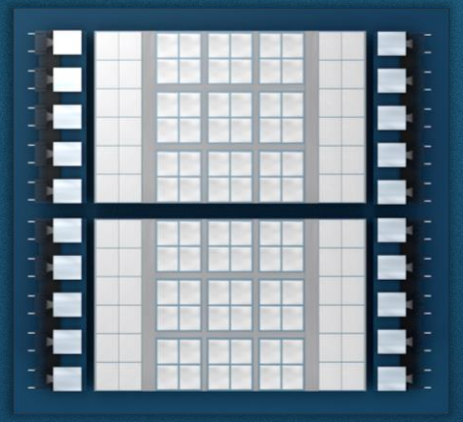
Package size:	~50x50mm^2
Silicon area:	~100mm^2
# of dies:	1
Transistor density:	~0.5M/mm^2

STATE-OF-THE-ART
AI GPU

PCF: ~32,000

Package size:	2X
Silicon area:	160X
# of dies:	118
Transistor density:	~200X

FUTURE
System-in-Package



PCF: >600,000

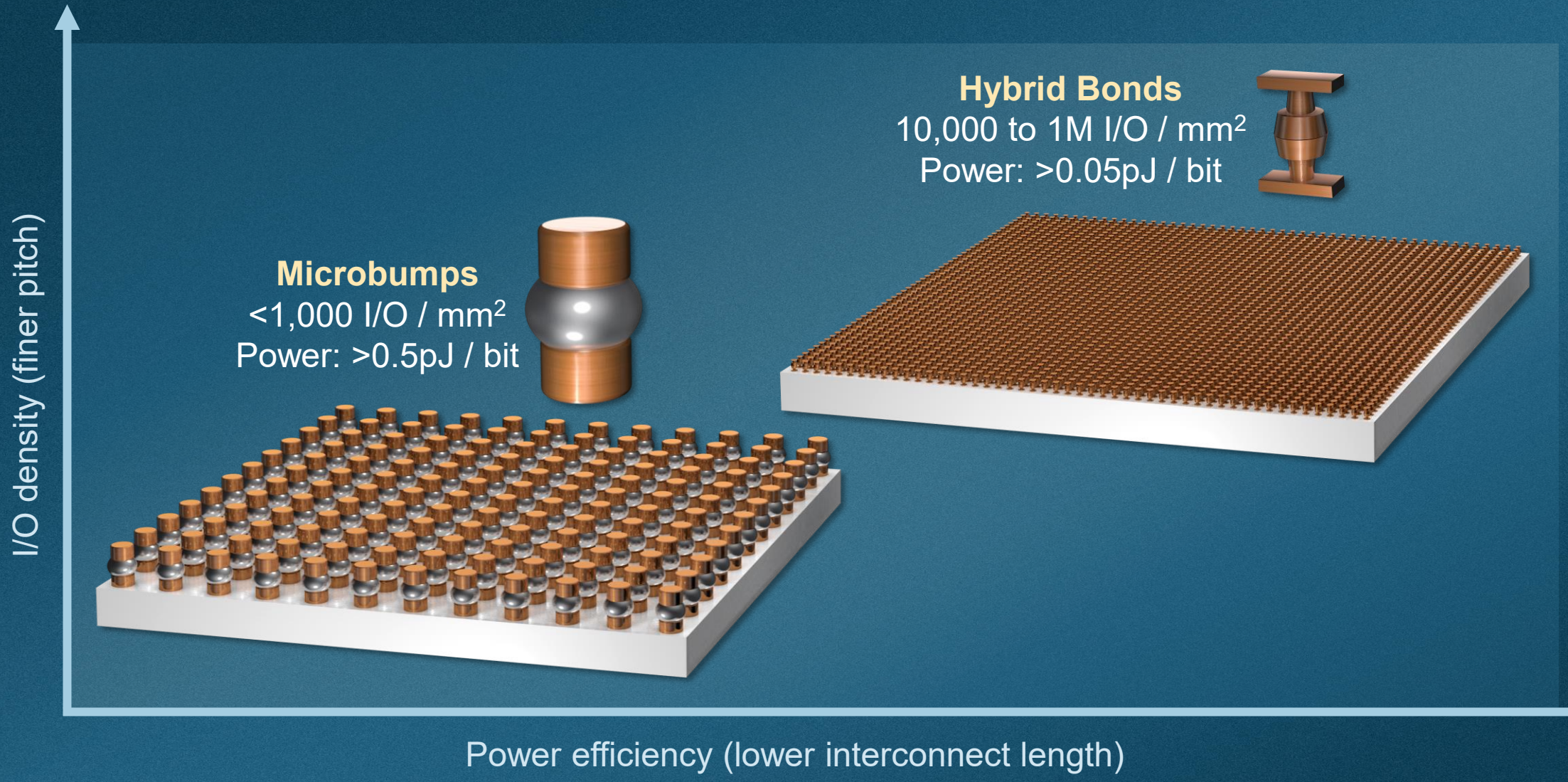
Package size:	9X
Silicon area:	>>600X
# of dies:	>400
Transistor density:	>1,000X

2000s **2020s** **Future**

Exponential Increase in Package Complexity Factor (PCF)*

* PCF = silicon area x transistor density

Hybrid Bonding for Lower Power and Higher Bandwidth



I/O: Input / Output

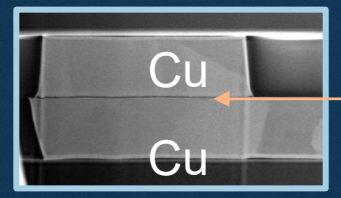
APPLIED MATERIALS

Hybrid Bonding Requires Co-Optimization and Integration

Conventional Flow

Simplified, for 2 wafers

Oxide CVD → Cu-pads + Dicing → Wet clean w/ carrier | Ambient | Wet clean w/o carrier | Ambient | Plasma activation | Ambient | UV release | Bonding | Ambient | Metrology



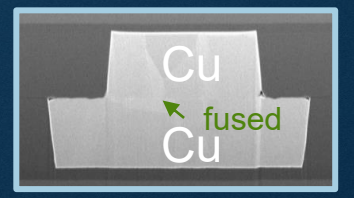
✗ Contamination risk

✗ Queue time issues

Integrated Flow

New Dielectric Material → Cu-pads + Dicing → Wet clean w/ carrier + Wet clean w/o carrier + Plasma activation + UV release + Bonding + Int. metrology

6 steps integrated in 1 tool



✓ Enhanced adhesion

✓ Improved yield

Applied Kinex™ Integrated Die-to-Wafer Hybrid Bonding System

Industry's First Integrated Die-to-Wafer Hybrid Bonding System

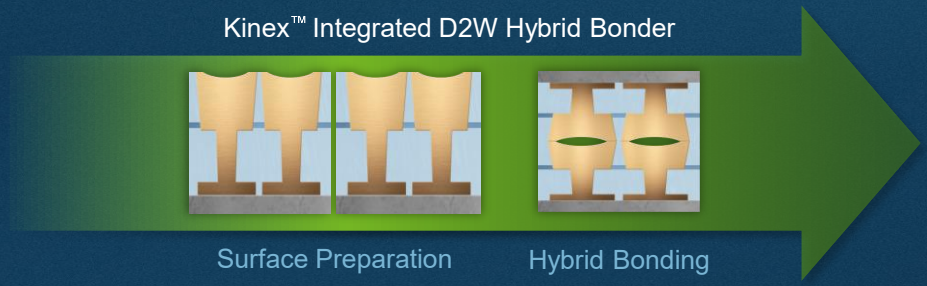
- ✓ Software-enabled chiplet management system supports traceability and binning requirements
- ✓ Integration maximizes yield through particle prevention, queue time optimization, and integrated metrology
- ✓ Besi's industry-proven bonder enable nanometer accuracy

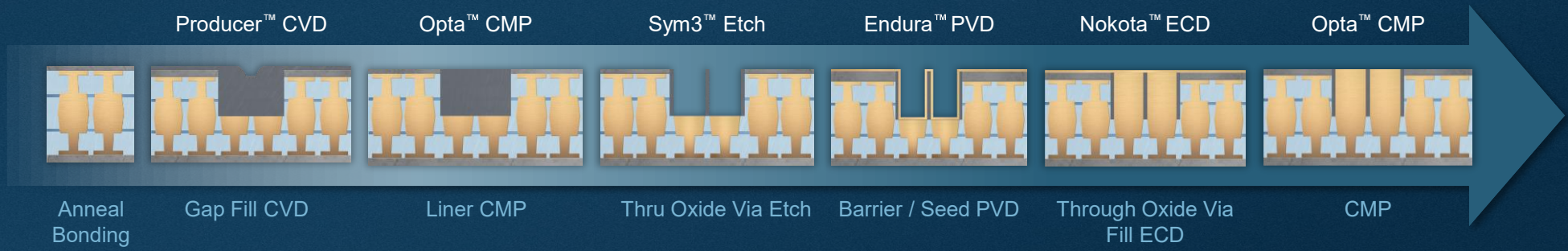
Tool of record at multiple leading-edge logic, memory, and OSAT customers
Qualified in production

Industry Leading End-to-End Portfolio of Hybrid Bonding Solutions

Co-optimized + Integrated

- Bonding CVD
- Warpage Modulation
- Pad Formation Etch
- Barrier / Seed PVD
- Cu Fill ECD
- CMP
- Wafer Singulation
- Surface Preparation
- Hybrid Bonding
- Anneal Bonding
- Gap Fill CVD
- Liner CMP
- Protective capping
- TOV Etch

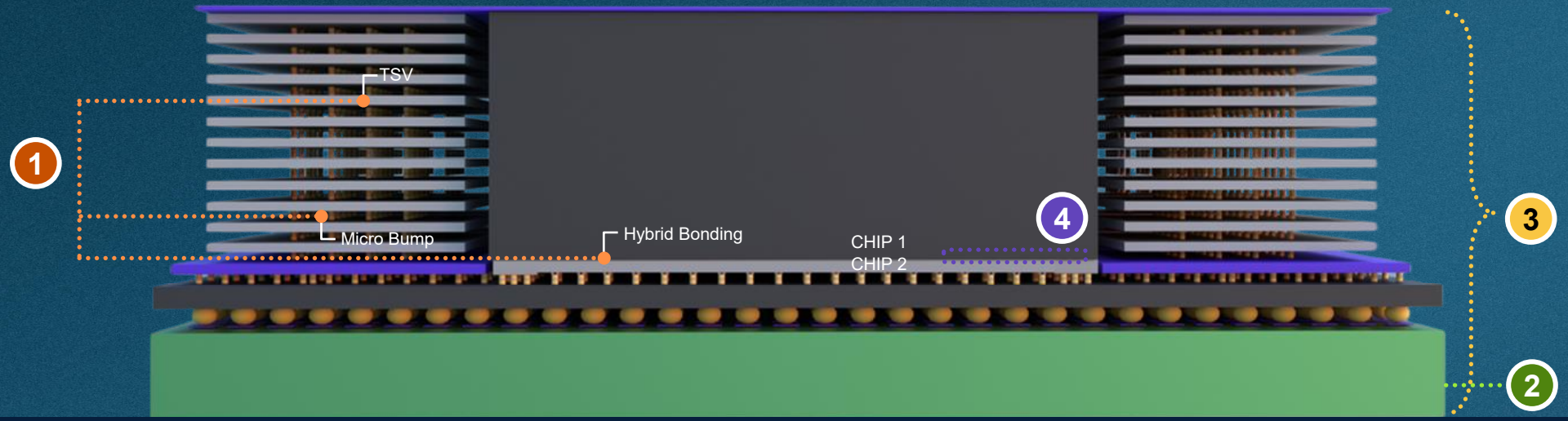




CVD: chemical vapor deposition
RDL: redistribution layer
PVD: physical vapor deposition

ECD: electrochemical deposition
CMP: chemical mechanical polishing
D2W: die-to-wafer
W2W: wafer-to-wafer

Applied's System-to-Materials Co-Optimization Platform
for Advanced Packaging Enablement



1 Micro Level Modeling

2 Advanced Substrate Modeling

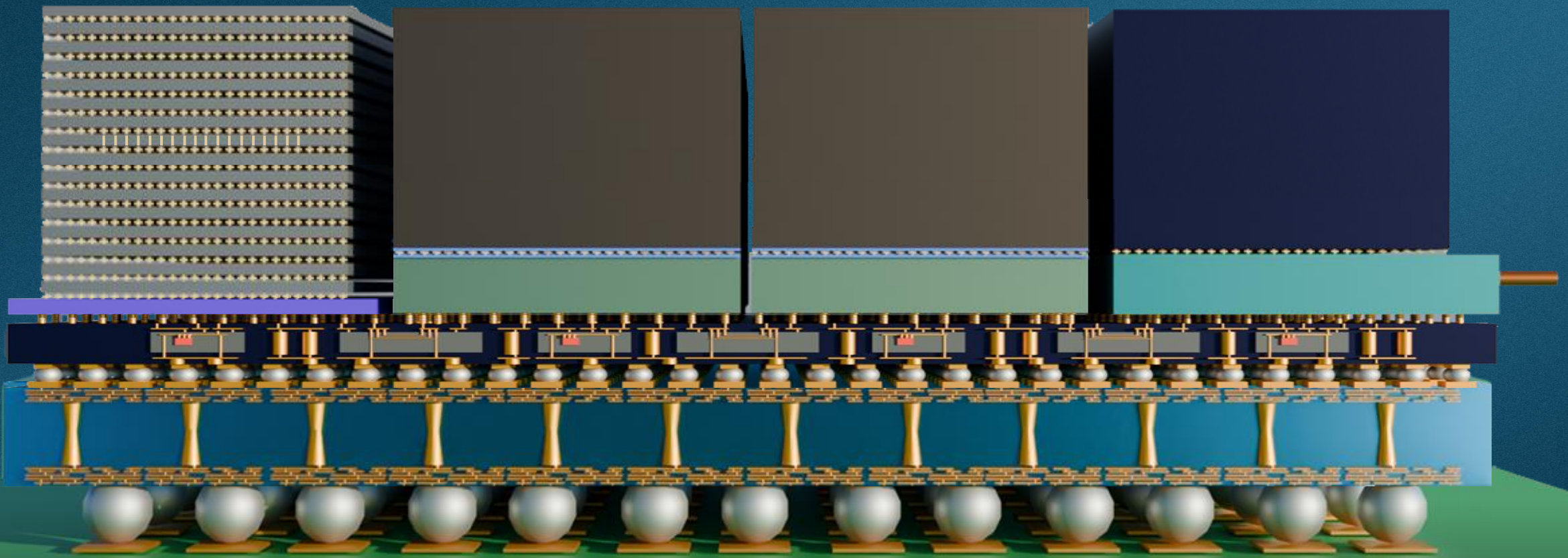
3 Packaging/System Level Modeling

4 Die Boundary Modeling

Advanced modeling capability to solve the unique materials engineering challenges for advanced packaging

Future Packaging Technology

HBM Hybrid Bonding + 3.5D IC Chiplets Stacking + Co-Packaged Optics + Large Interposers + Bridges + Passives + Panels + Glass



Applied's Broad Portfolio + EPIC Platform = Faster Packaging Innovation

Fab Enablement

R&D Acceleration

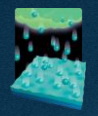
Mike Chudzik, Ph.D.

Vice President of Technology, Semiconductor Products Group

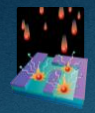
OCTOBER 7, 2025

R&D Acceleration Enablers

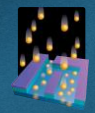
Largest Tool Portfolio
Process and Metrology



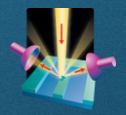
CREATE:
CVD, PVD, ALD, Plating, Epitaxy, Selective Deposition



SHAPE:
Etch, CMP, Sel. Removal, Pattern Shaping



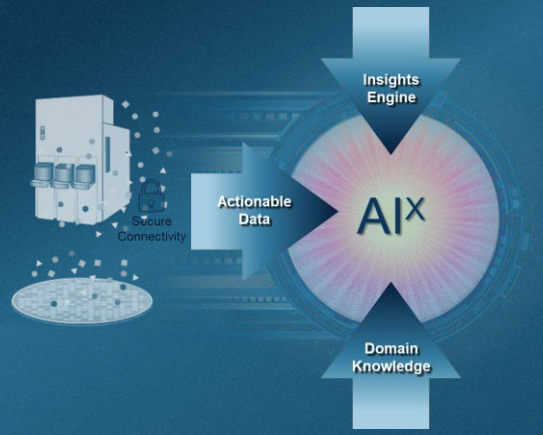
MODIFY:
Implants, Thermal, Treatments, Oxidation



ANALYZE:
Optical, E-Beam, CD-SEM, Defect Review

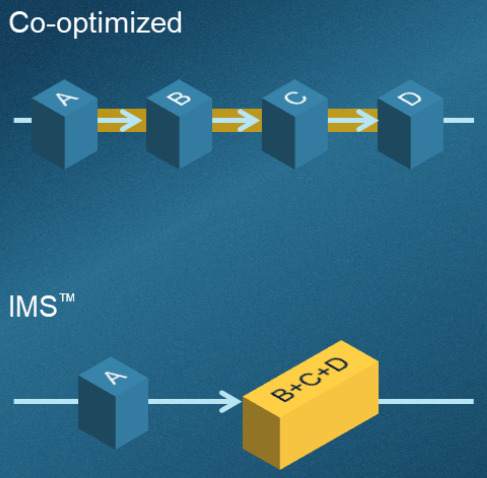
In-line metrology, process, and digital tool capabilities compress learning cycles

Digital Tools: AI^{X}™



AL/ML analytics and digital twins for R&D speed and process windowing

Co-Optimized Modules



Foundational building blocks beyond unit processes providing turnkey solutions

EPIC™ Platform

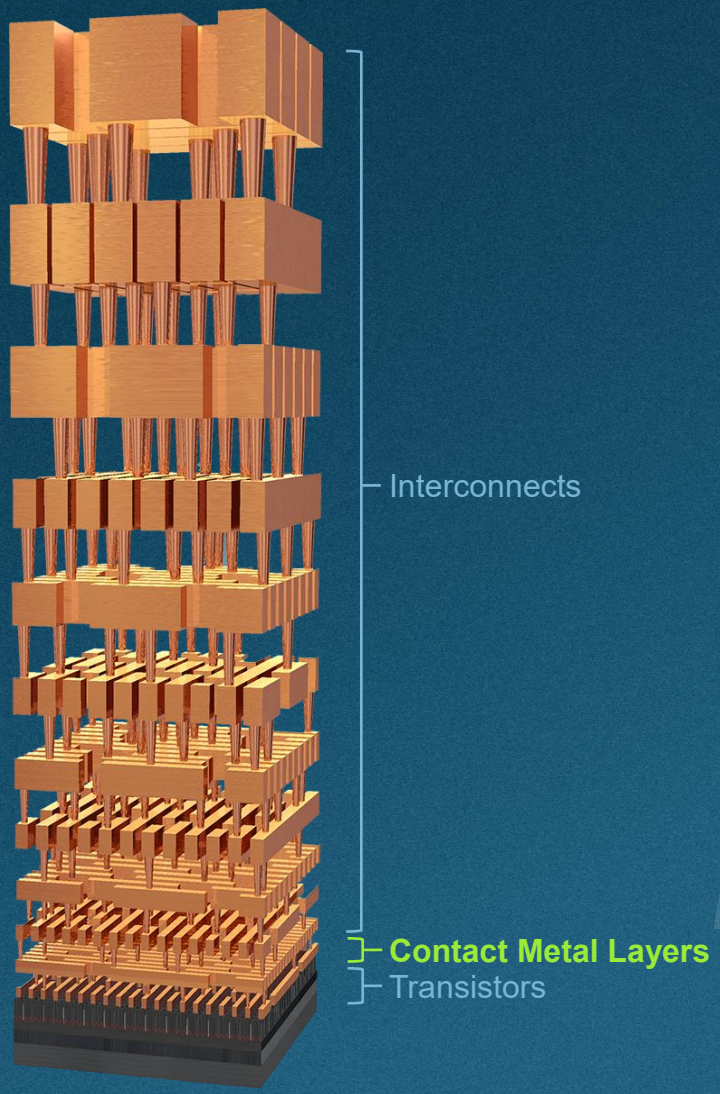
Drive higher velocity co-innovation to accelerate R&D

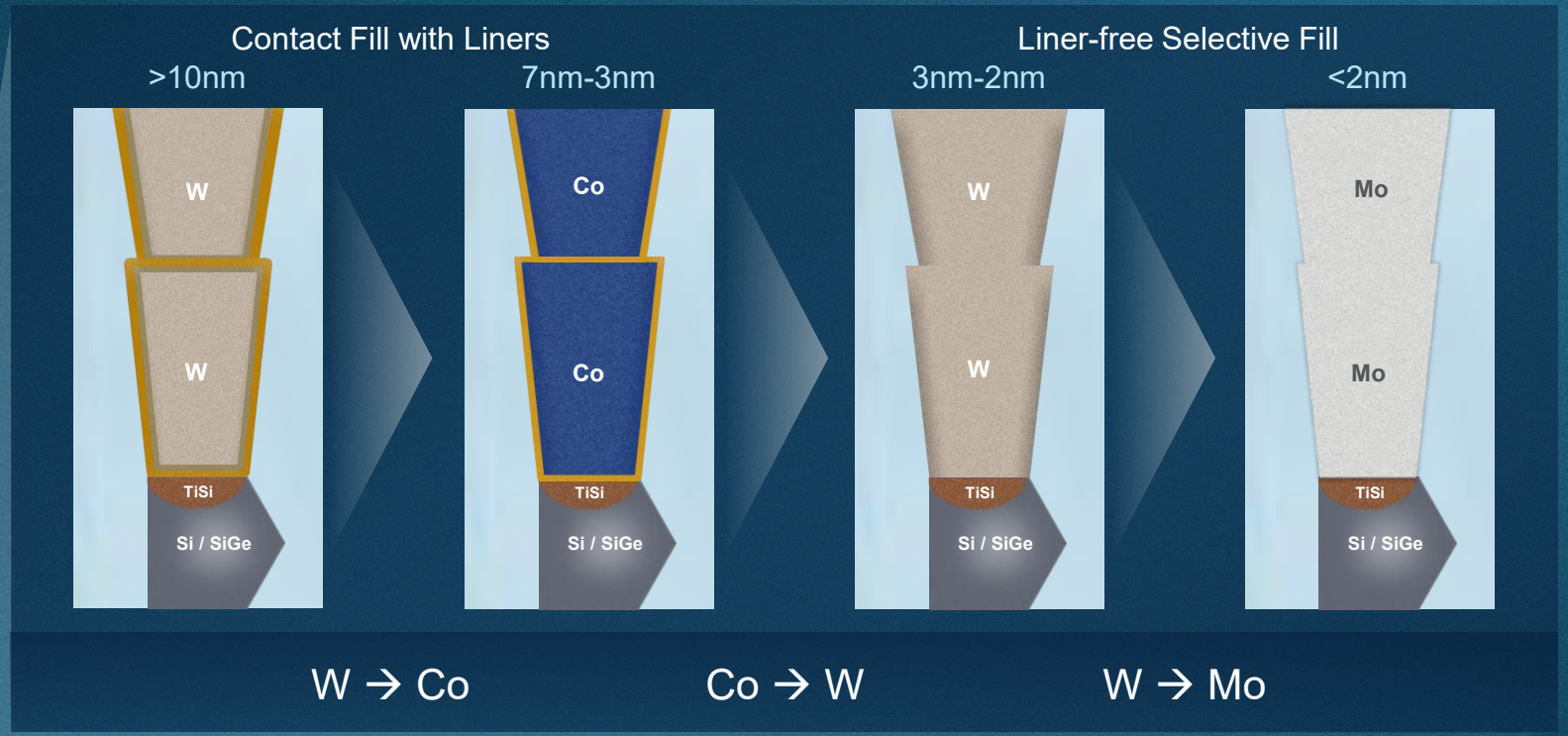
CVD : chemical vapor deposition
PVD : physical vapor deposition
ALD : atomic layer deposition

CMP : chemical mechanical planarization
AI^{X} : Actionable Insights Accelerator
IMS : Integrated Material Solution

APPLIED MATERIALS

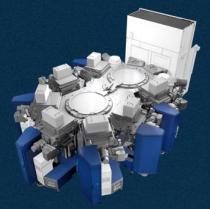
From Tungsten to Moly Leadership in Contact Scaling





1 Trillion contacts across a 300mm wafer

Mo Contacts: Process + Metrology + Digital Tools for Speed

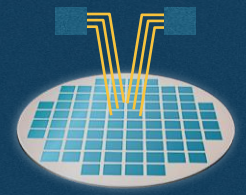


Endura™ PVD

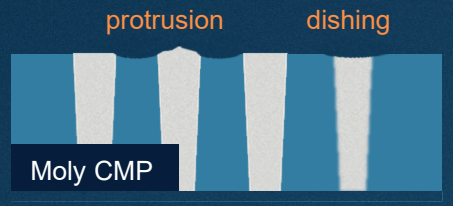
Cross-Sectional
TEM~1-2 sites

Opta™ CMP

Cross-Sectional
TEM: ~1-2 sites

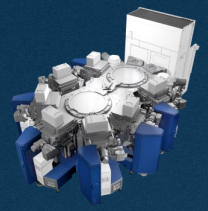


Electrical Testing:
>1,000 sites



(Weeks Later)

TRADITIONAL LEARNING CYCLE



Endura™ PVD

PROVision™ 10
>10,000 sites

AIX Digital
tools

Opta™ CMP

PROVision 10
>10,000 sites

AIX Digital
tools

ACCELERATED LEARNING CYCLE

Close the Loop in
Hours versus Weeks

Co-Optimized Modules to Save Months of Development Time

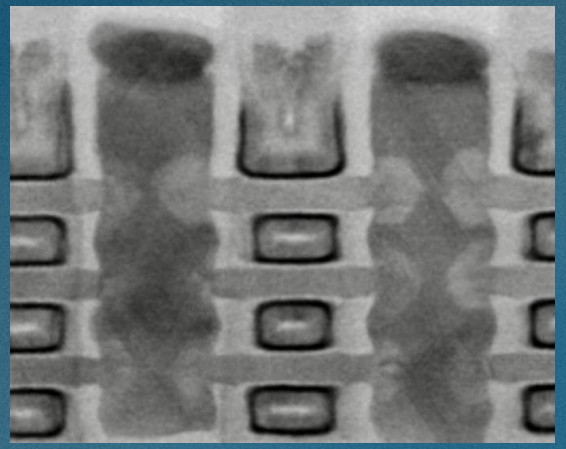
Device Specification

Tool Demo / Selection → Tool Order / Build → Tool Startup and Qualification → Module Development at Customer Site → Production Ramp

Early –Access Technologies → Module Development at Applied Materials → Module Demo with Customer

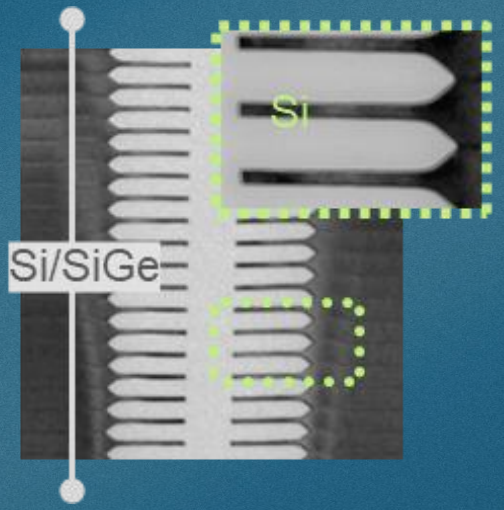
~30% TIME SAVED

LOGIC
GAA Contact Module



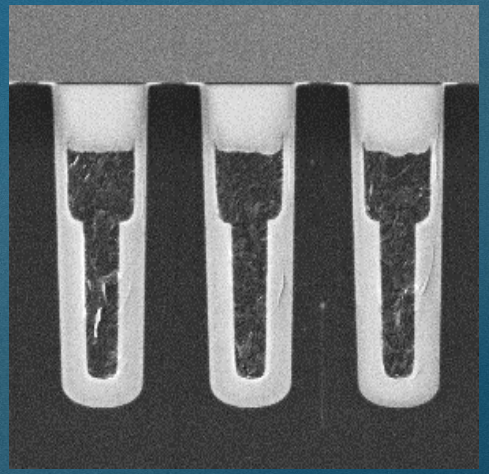
~20 STEPS

MEMORY
3D DRAM: Si Channel



~25 STEPS

ICAPS
Si MOSFET Split Gate Module



~15 STEPS

ICAPS: IoT, Communications, Automotive, Power, Sensors

APPLIED MATERIALS

Applied EPIC Platform – IP Secure High Velocity Co-Innovation

GLOBAL NETWORK OF CAPABILITES

Customer-like Test Vehicles and Reticles

Fast turn around short-loop test vehicles

- >200 test vehicles for Logic, Memory, ICAPS
- Thousands of integrated wafers/month

IP Security

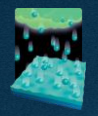
Locked down recipes, locked down integration flows, wafer RFID tracking, and dedicated SEM/TEM folders

- MES system: customer dedicated routes and recipes
- Secured customer reticles and TEM/SEM database
- RFID traced customer wafer/samples

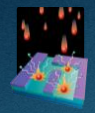
META: Materials Engineering Technology Accelerator
APDC: Advanced Packaging Development Center
ICAPS: IoT, Communications, Automotive, Power, Sensors

R&D Acceleration Enablers

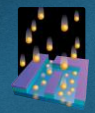
Largest Tool Portfolio
Process and Metrology



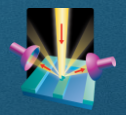
CREATE:
CVD, PVD, ALD, Plating, Epitaxy, Selective Deposition



SHAPE:
Etch, CMP, Sel. Removal, Pattern Shaping



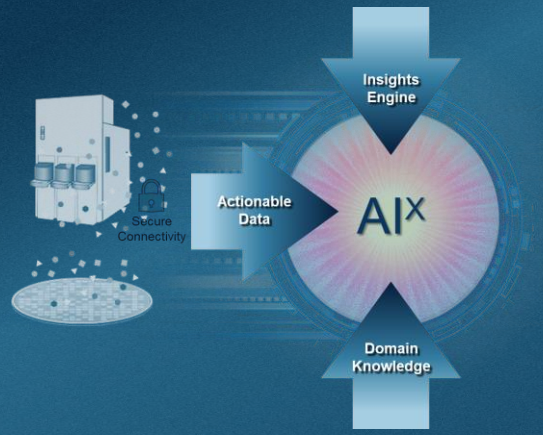
MODIFY:
Implants, Thermal, Treatments, Oxidation



ANALYZE:
Optical, E-Beam, CD-SEM, Defect Review

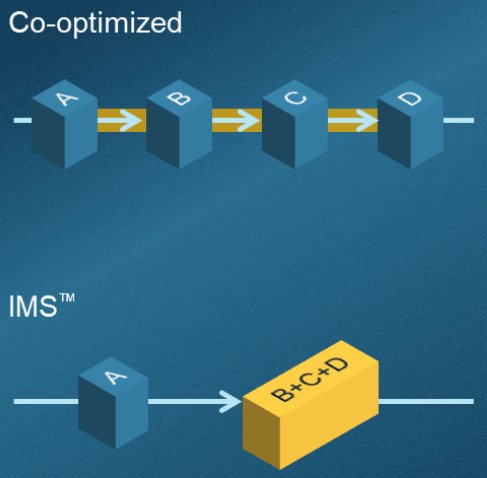
In-line metrology, process, and digital tool capabilities compress learning cycles

Digital Tools: AI^{X}™



AL/ML analytics and digital twins for R&D speed and process windowing

Co-Optimized Modules



Foundational building blocks beyond unit processes providing turnkey solutions

EPIC™ Platform

Drive higher velocity co-innovation to accelerate R&D

CVD : chemical vapor deposition
PVD : physical vapor deposition
ALD : atomic layer deposition

CMP : chemical mechanical planarization
AI^{X} : Actionable Insights Accelerator
IMS : Integrated Material Solution

APPLIED MATERIALS

Fab Enablement

Manufacturing Ramp Acceleration

Steve Frezon

Vice President, Customer Services and Support, Applied Global Services

OCTOBER 7, 2025

High Velocity Commercialization

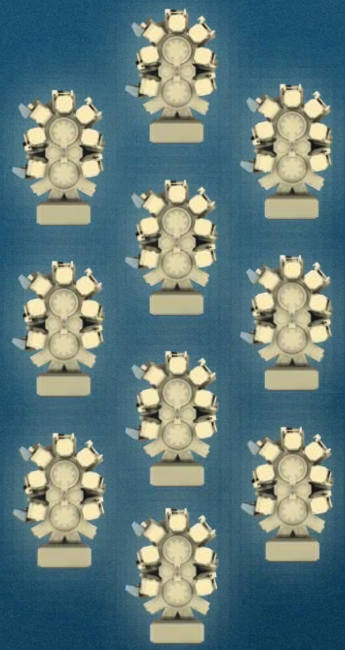
TIME TO MARKET

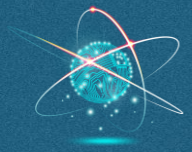
HIGH VELOCITY CO- INNOVATION

HIGH VELOCITY COMMERCIALIZATION

R&D | RAMP | HVM

Golden Tool



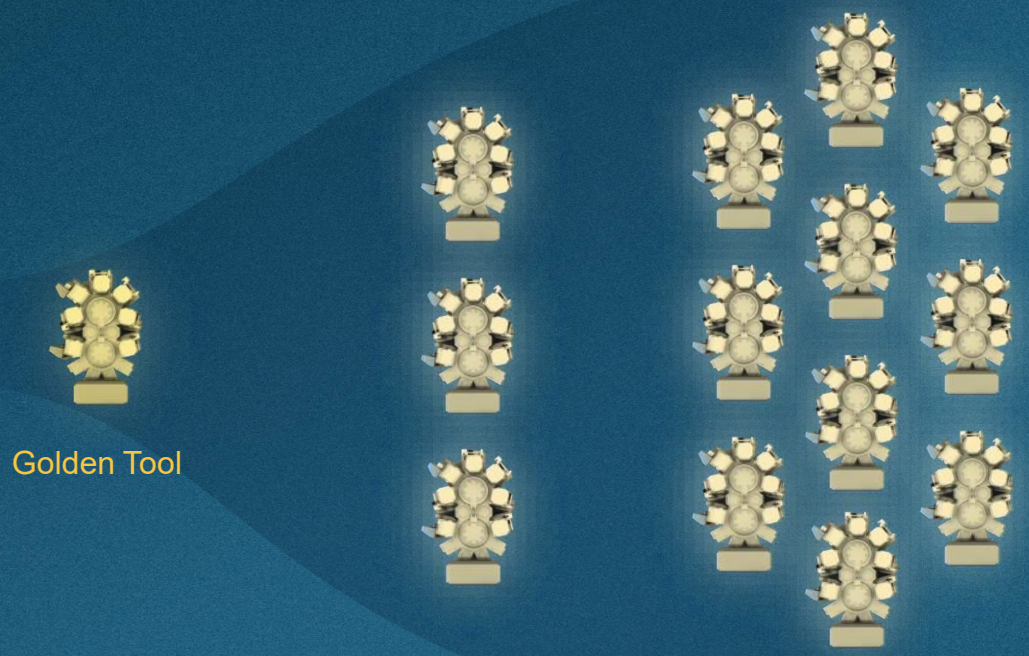


Atomic-level Precision Needed at Industrial Scale

Accelerating Time to Market

TIME TO MARKET

R&D | RAMP | HVM

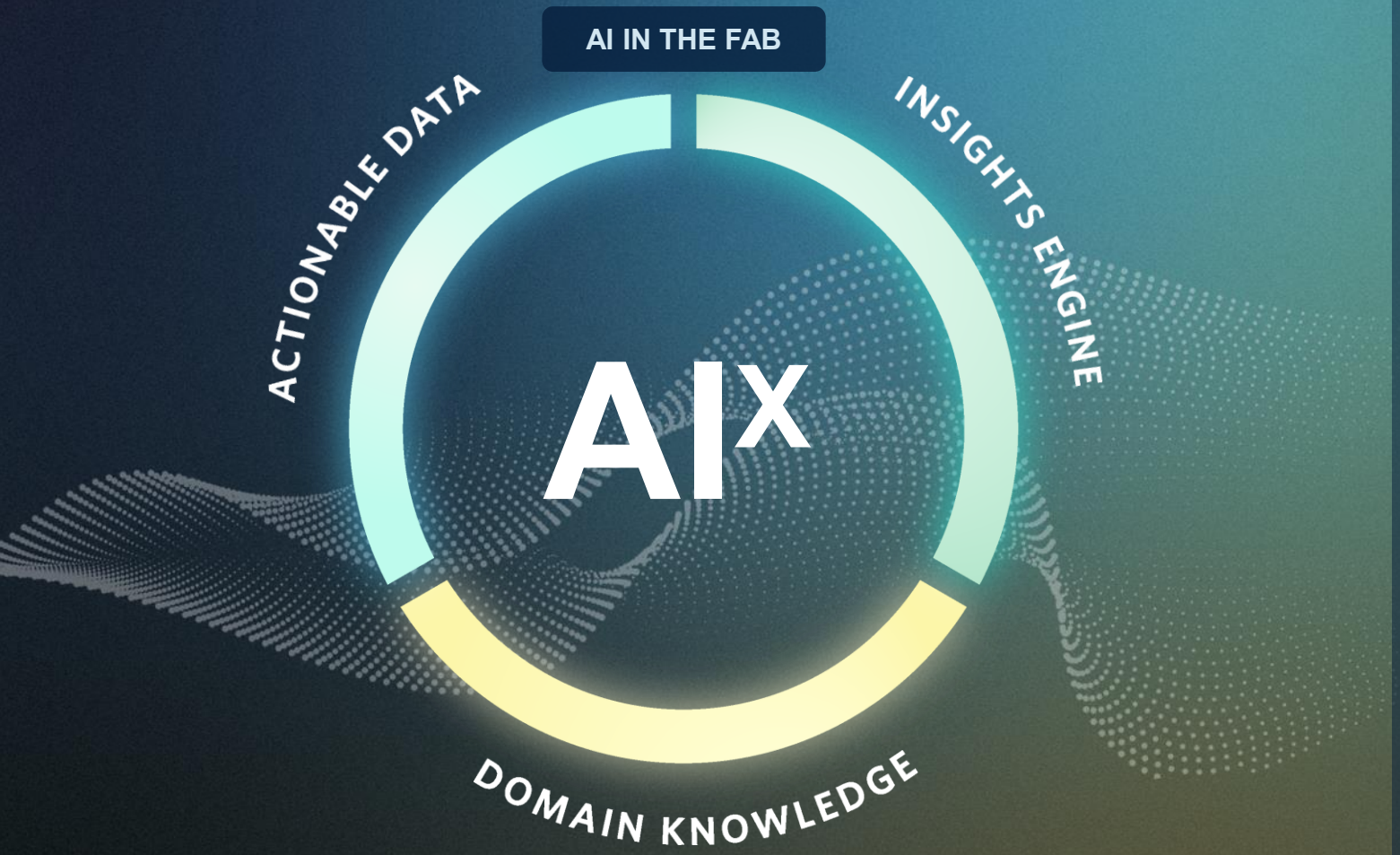


Golden Tool

- YIELD
- OUTPUT
- COST

Atomic-level Precision Needed at Industrial Scale

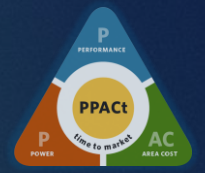
Service Innovation – Accelerating Time to Market



Actionable Insight Accelerator (AI^X) Platform

ACCELERATE

Results



	Applied Solutions
R&D Time to qualify Process window	AppliedPRO™
Ramp Time to match Yield optimization	CrossMatch™
HVM Yield Output Cost of ownership	Defect Expert System FleetOptimizer™ Predictive Maintenance

Service Innovation - First Time Right

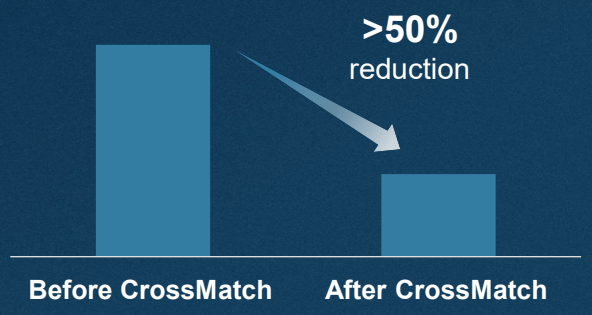
CrossMatch™

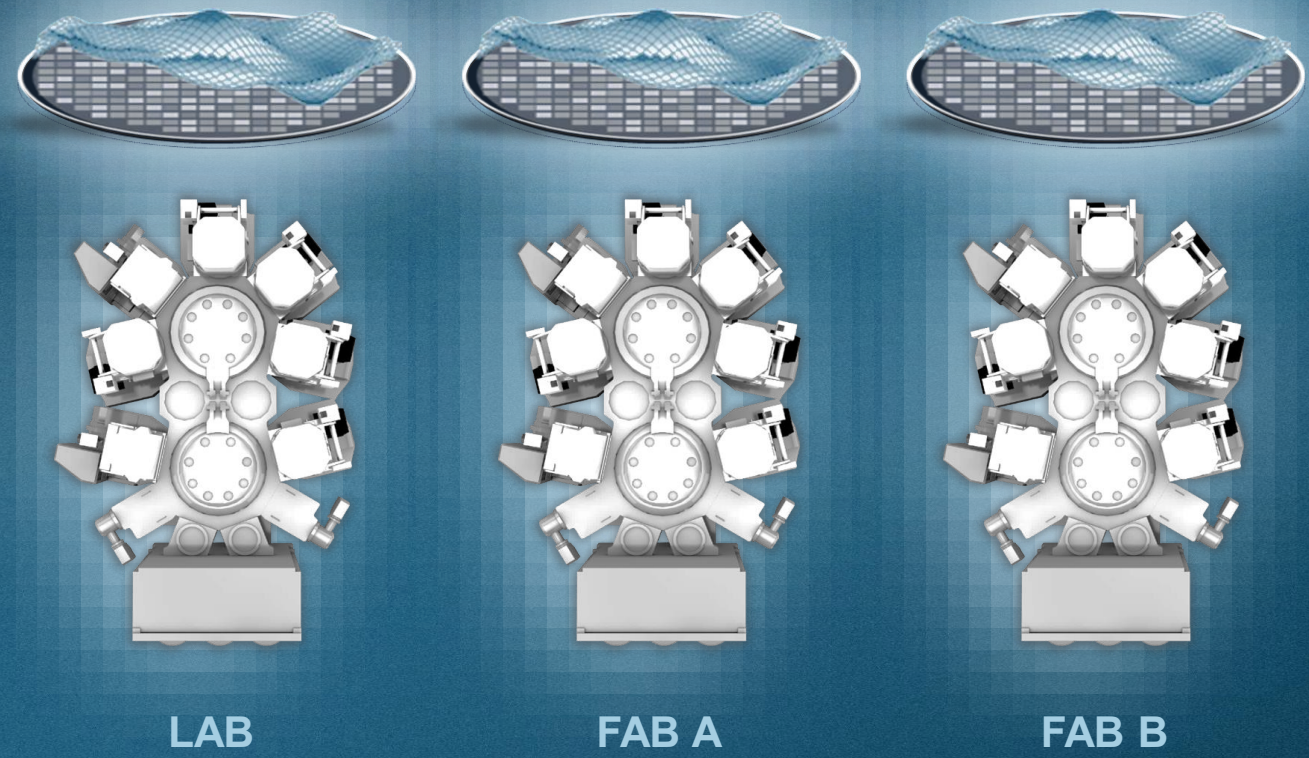
Matching at angstrom level precision

KEY PARAMETERS

Critical Dimensions	Linearity
Uniformity	Resistance
Profile Angle	Stress
Zonal Profiles	Defects

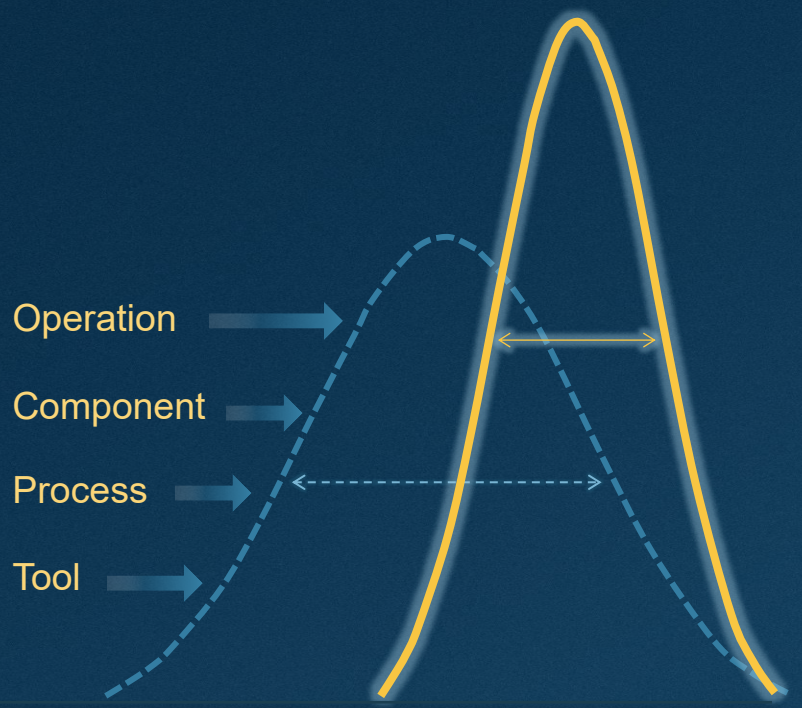
TIME TO MATCH





Accelerating Performance & Yield

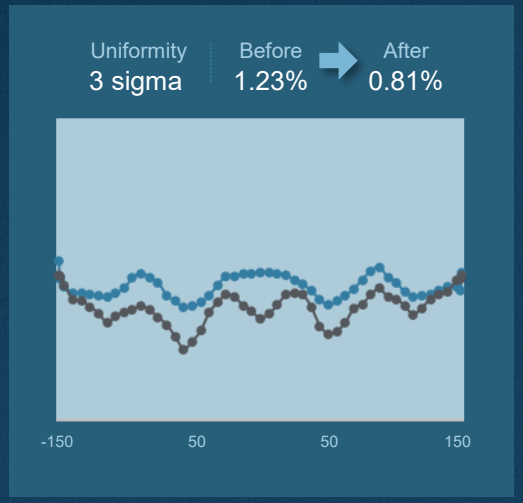
Service Innovation - Reduce Variability for Higher Yield & Output



Components

EPI

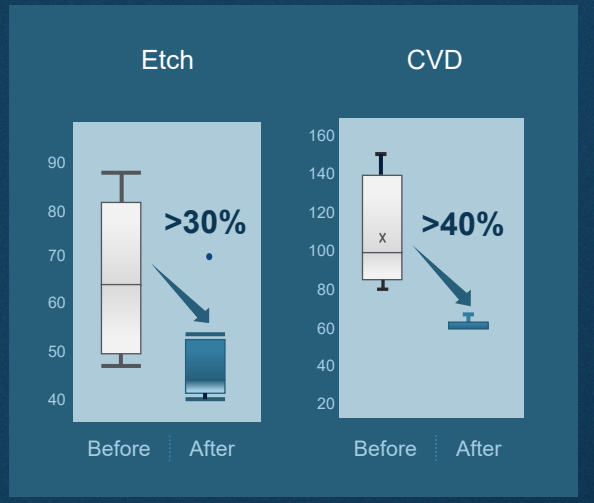
>30% Uniformity Improvement



PM Engineering

Etch & CVD

Green-to-green Improvement



AppliedPRO™

CVD

Centering Process Window

Enabling Higher Performance

Service Innovation – Increasing Output

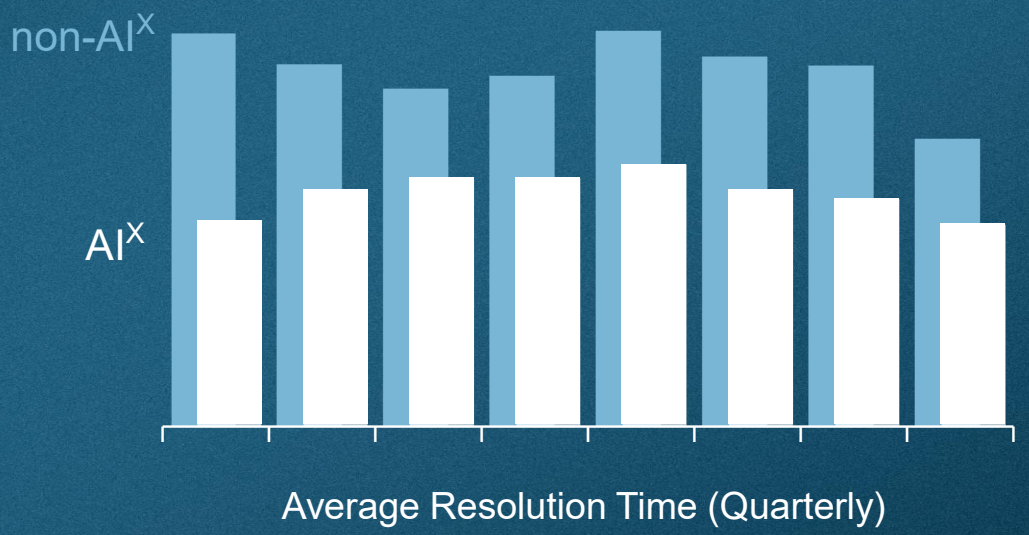
AI^X –CONNECTED TOOLS → HIGHER OUTPUT

Global Network

SECURE CONNECTIVITY

30%

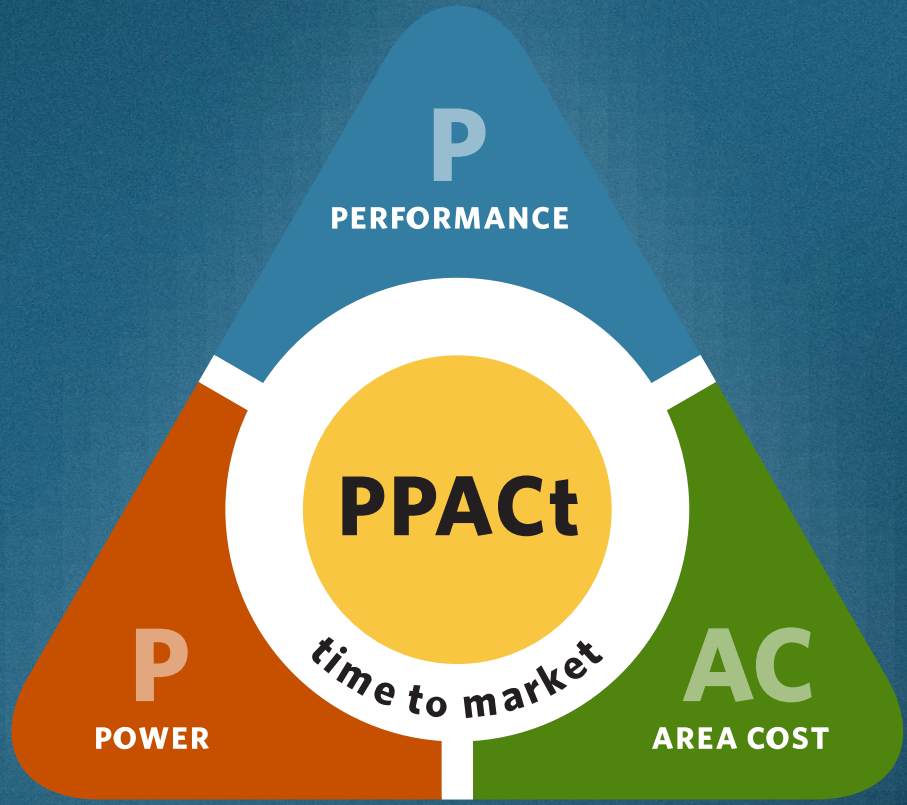
FASTER RESOLUTION



Accelerating time to resolution

Accelerating Commercialization Together

Faster Time to Market in the AI Era



Growing our Opportunity and Share

Prabu Raja, Ph.D.

President, Semiconductor Products Group

OCTOBER 7, 2025

Strong Global Fab Investments Outlook

Active Fab Projects*

>100 Worldwide

*Projects under operation / equipping / construction / planning

Device Inflections Enabled by Materials Engineering

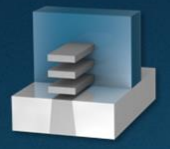
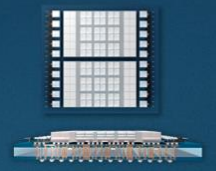
Semi Devices Foundational for Energy Efficient Performance

- Leading-edge Logic
- High-performance DRAM
- High-bandwidth DRAM
- Advanced Packaging
- Power semi (ICAPS)

ICAPS: Internet of Things, Communications, Automotive, Power and Sensors

Applied Materials External

New 3D Architecture Inflections Offer Big EEP Improvements

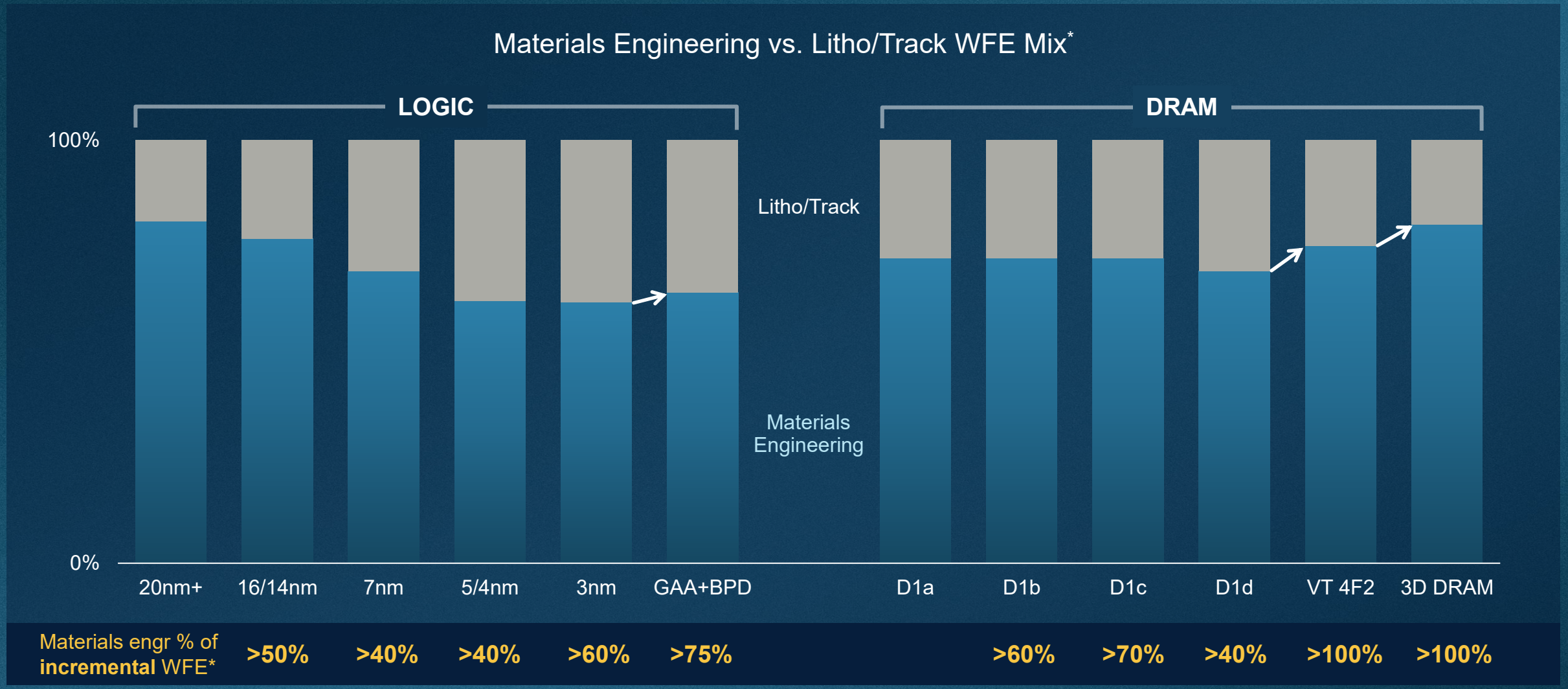
AI Leading-edge Logic		AI DRAM: HBM + Leading Edge			AI Sys. Integration
					
GAA Transistor	Backside Power	High Bandwidth Memory	Vertical Transistor	3D DRAM	Advanced Packaging
30% ↓ power, 15% ↑ performance	30% ↑ density ↑ 10% performance	Bandwidth +1,000%	EEP +15%	EEP +15%	1000x ↑ IO / mm² 10x lower pJ / bit ↓

Helping deliver **10,000X EEP improvement** by 2040

IO: input/output, EEP: energy-efficient performance

Applied Materials External

Expect Materials Engineering to Increase within WFE Mix

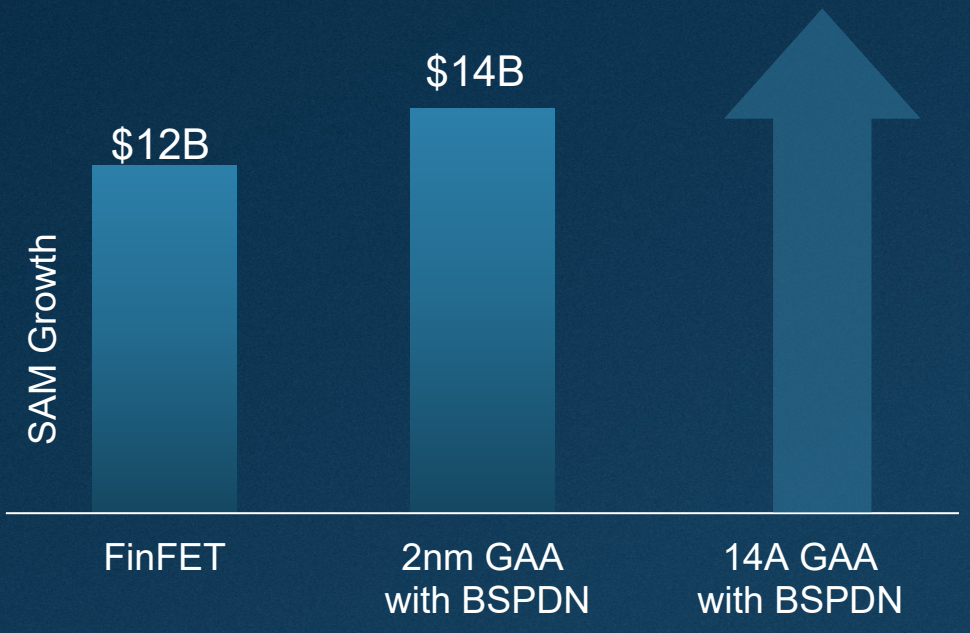


Source: Applied Materials analysis
* Materials engineering vs litho/track WFE mix & ME as % of incremental WFE exclude cleans and process control
Materials engineering (ME) % of incremental WFE = (ME WFE spend on new node – ME WFE spend on prior node) / (WFE spend on new node – WFE spend on prior node)

Device Inflection Growth Opportunities

LEADING-EDGE LOGIC

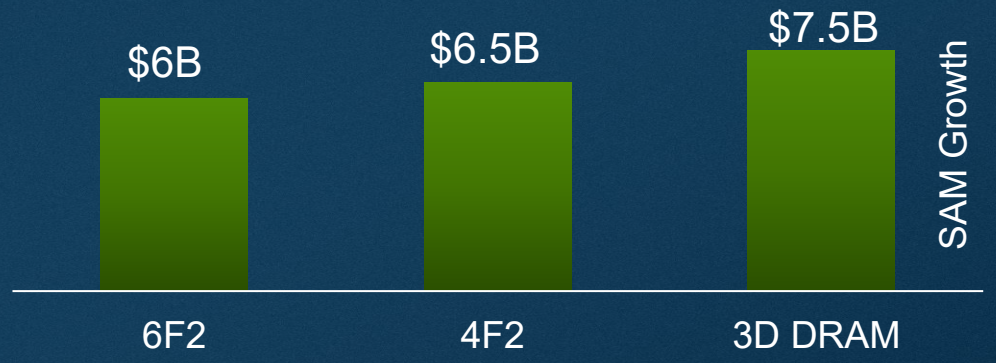
Several pts share gain | +30% Revenue Oppty.*



ADVANCED DRAM

Several pts share gain | +30% Revenue Oppty.*

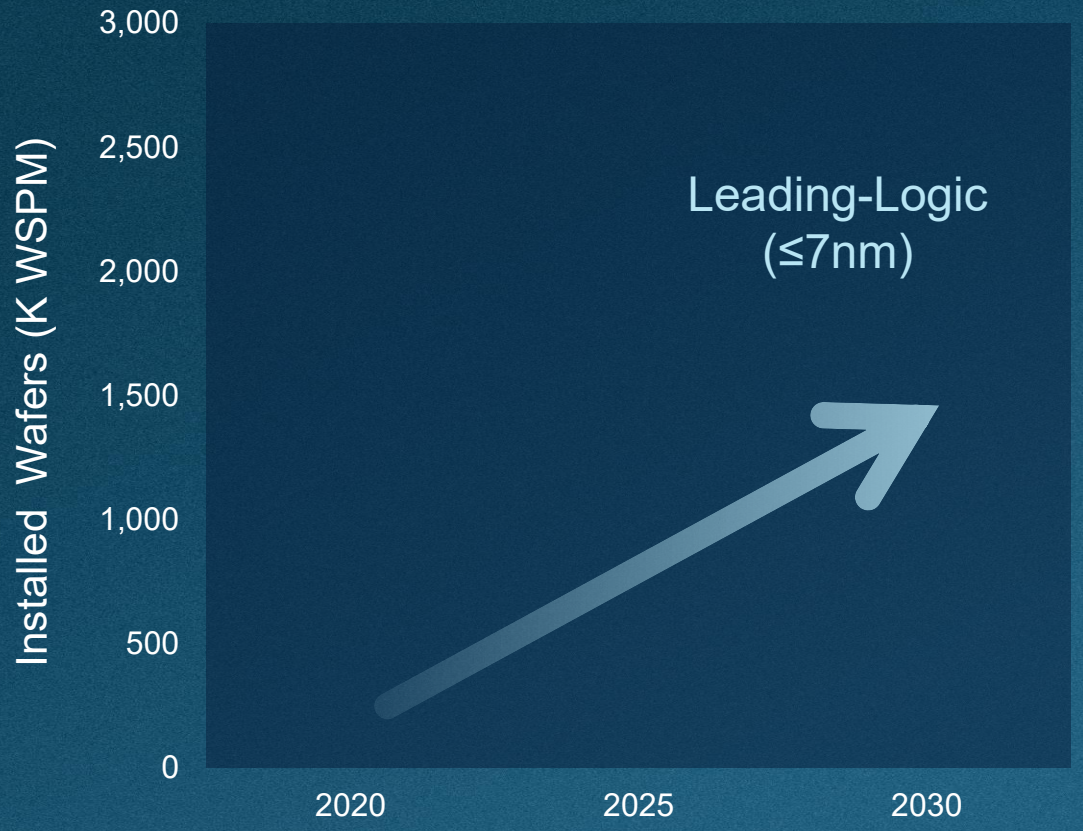
+ 10pts share in over 10 years



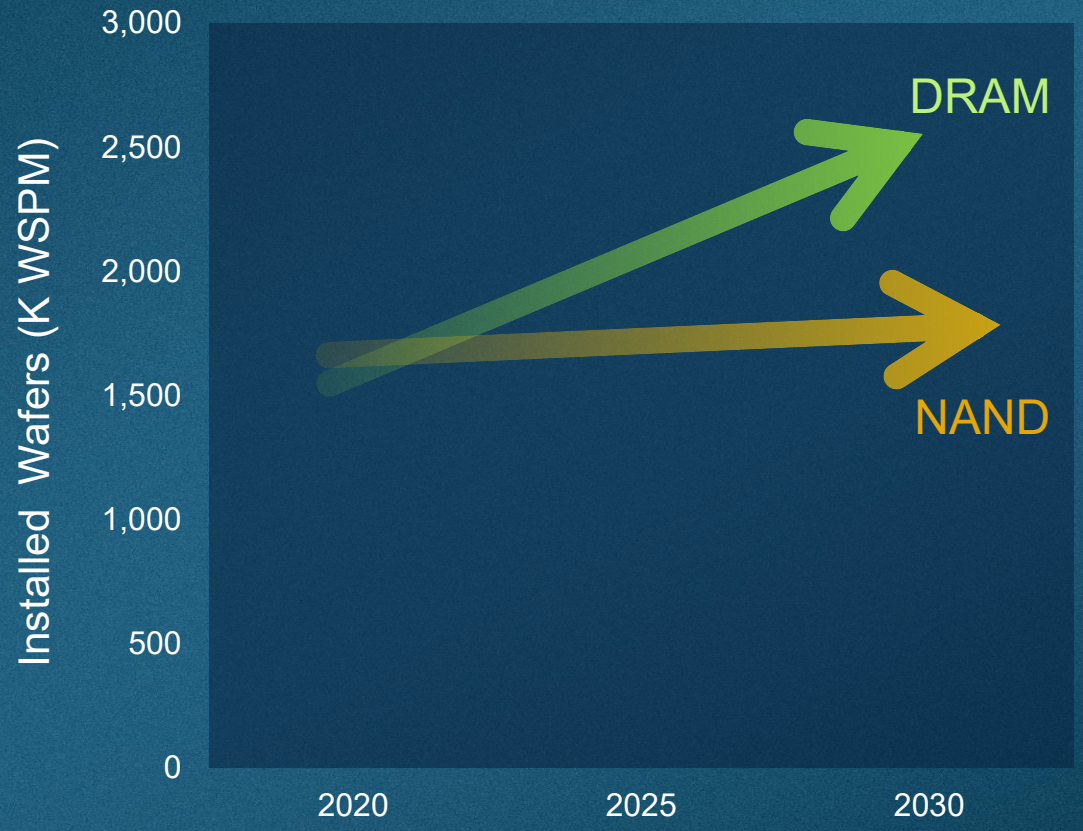
Benefiting from strong market growth AND
Positioned for share gains to **50% SAM share** at new inflections

SAM = Served Addressable Market per 100k wafer starts per month capacity.
GAA: gate all around, BSPDN backside power delivery
*Logic: FinFET to GAA; DRAM: 6F2 to 3D DRAM; for the equivalent fab capacity (per 100K wafer starts per month)

Strong Wafer Starts Growth Expected for Advanced Logic and DRAM



New additions at 3nm and below nodes

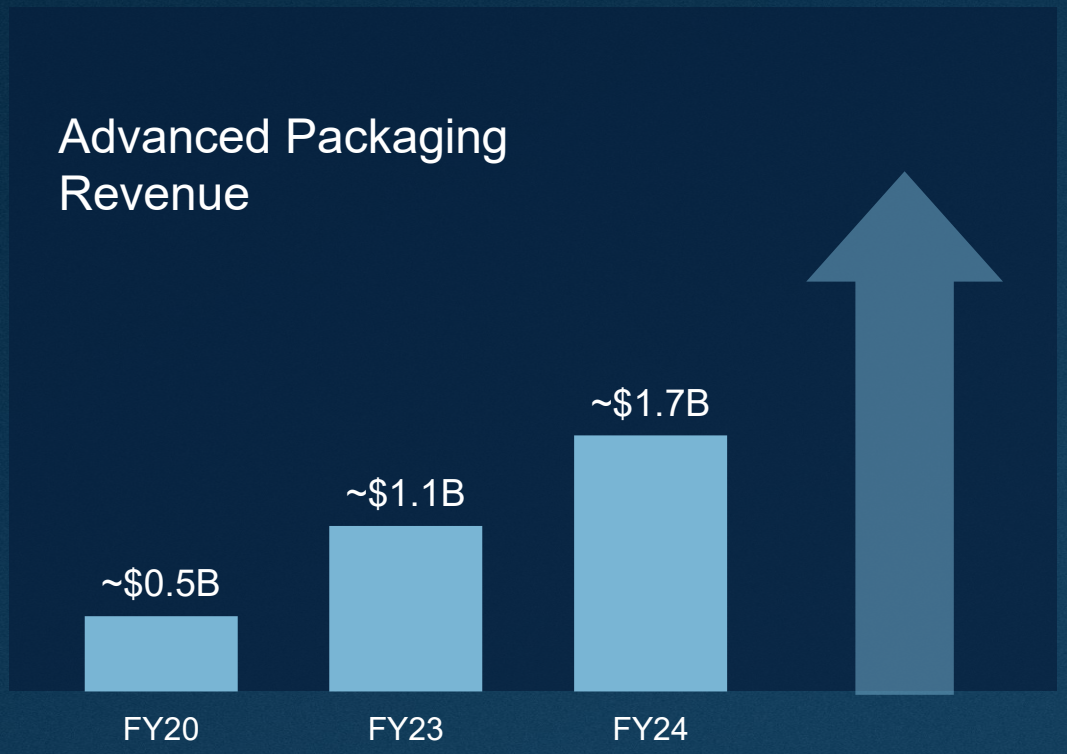


DRAM: Expanding with greenfield + transitions

NAND: Primarily technology transitions

Applied Materials estimates

Packaging Offers Key Growth Opportunity



Industry's broadest and most connected heterogeneous integration portfolio

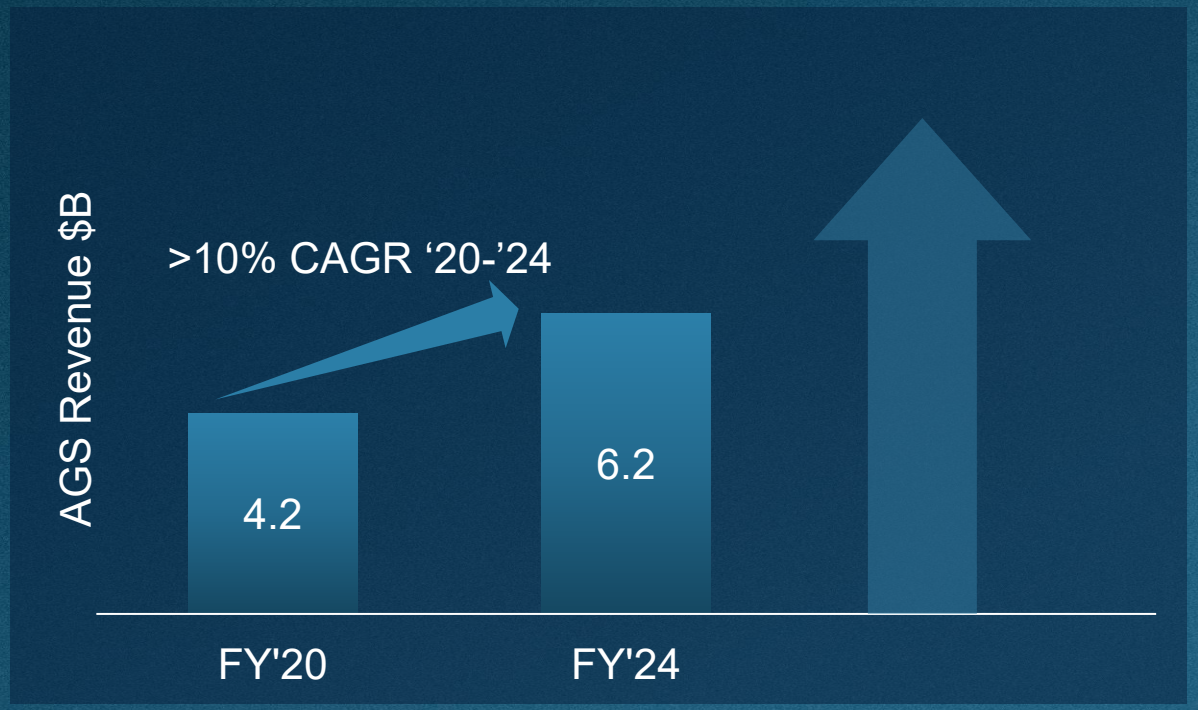
Extends Applied's leadership in on-chip wiring to off-chip wiring (#1 overall, #1 in HBM)

Building a leadership portfolio for emerging hybrid bonding and panel technologies

Applied's display expertise helps accelerate panel ecosystem

Applied Materials estimates

Sustained, Profitable Growth through PPACt Services



>2/3 of core AGS revenue from subscriptions

>18K tools under Service Agreements

>90% Renewal Rate

Helping customers manage technology complexity in the AI-era drives growth for AGS

Applied Well Positioned to Grow with AI Mega Trend

↑ Market from AI silicon content

>100 active fab projects
↑ Wafer starts

×

↑ Nodal SAM from device inflections

↑ Logic and DRAM SAM

×

↑ Share, service by solving key HVPs

Several pts share
AGS growth

- Unique connectivity strategy (addresses high technology complexity)
- High velocity co-innovation with EPIC
- Favorable device mix exposure (benefiting leadership areas)
- Growing installed base + PPACt services (incl. yield, variability control)

2025 SEMICON WEST

Technology Breakfast

APPLIED MATERIALS